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Low Power Adders for Efficient Image Processing Applications

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Abstract

In the world of digitalization, low-power circuits are necessary for building fast operating processors. Additionally, low-power circuits consume less energy and the lifetime of the electronic devices can extended to the maximum. Adders are significantly used in digital image processing techniques and for many Very Large-Scale Integration (VLSI) applications. Due to this, demand for creating efficient adders has become high in recent years. Using approximate adders is much more convenient than exact adders and the results of approximation adders are better than exact adders. Approximation adders can be executed for many signal-processing applications and are mainly considered for image-processing applications. SESA and SEDA are very good in providing efficiently lower energy when compared to other mirror adder circuits and are cost-efficient. Improvements and further extensions of the proposed model can easily make for building efficient microprocessor chips and these adders are used in next-generation electronic devices.

Keywords: *Very Large-Scale Integration, approximation, adders, low power, efficiency, microprocessor, image processing.*

1. Introduction

Due to the developments of new generation microprocessor chips, it is necessary to improve microelectronic chips with high reliability and Printed Circuit boards (PCB) that comply with enhanced circuit fabrications. The Arithmetic Logic Unit (ALU) plays an important role in creating enhanced electronic circuits for microprocessors. An ALU is a key component of a computer's central processing unit (CPU) [1]. Its primary function is to perform arithmetic and logical operations on binary data. These operations are fundamental to the execution of computer programs and the processing of data. The arithmetic unit is a part of the ALU that handles arithmetic operations such as addition, subtraction, multiplication, and division. It consists of adders and multipliers capable of performing binary calculations. The logic unit handles logical operations, including bitwise operations like AND, OR, and XOR as well as other operations like comparisons and shifting. After this control unit manages the operation of the ALU, ensuring that the correct operation is performed based on the given instructions. The ALU operates based on instructions provided by the CPU. These instructions specify what operation should be performed (e.g., addition or bitwise AND) which operands to use (source data), and where to store the result (destination). The ALU retrieves the operands from registers or memory, performs the specified operation, and stores the result. ALU design can vary depending on factors like the computer's architecture, the desired performance, and the available technology. Modern CPUs often have highly optimized ALUs to handle a wide range of operations efficiently. The performance of an ALU is crucial for the overall speed and efficiency of a CPU. Improving ALU design and performance is a constant focus in computer architecture research. ALU is a fundamental component of a computer's CPU and is responsible for carrying out arithmetic

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Page No: 19 - 23
https://irjaeh.com

and logical operations on binary data [2]. It plays a critical role in executing instructions and processing data in computer programs. Moreover, it makes it a core element of digital computing. Adders play a major role in ALU and it is an important basic unit for developing ALU architecture. Adders are fundamental digital circuits or components used in computer systems and digital electronics to perform arithmetic operations, primarily addition. They are essential building blocks for various computations and data processing tasks. There are different types of adders- half adders, full adders, ripple carry adders, carry skip adders, logged-stone adders, and so on. These various types of adders offer different trade-offs in terms of speed, complexity, and area utilization. Engineers choose the most suitable adder design based on the specific requirements of their digital circuits and applications. Speed, efficiency, and low power energy are often critical considerations in selecting an adder type, especially in high-performance computing systems and processors. Adders are mainly used in real-time image processing applications and DSP processors. Exact adders cannot give accurate and dynamic results. Many processor applications cannot use exact adders for their operations. Approximation adders are necessary for creating efficient microprocessors. Approximation adders are a class of digital adder circuits designed for energy-efficient and high-speed arithmetic operations with approximate results. Approximation adders are commonly used in low-power and high-performance computing systems as well as in applications such as image and signal processing. Approximation adders perform approximate arithmetic, meaning they sacrifice some level of accuracy to achieve benefits like reduced power consumption and faster operation. They are often used in applications where a high degree of precision is not necessary, such as multimedia processing, sensor data fusion, or machine learning. One of the main advantages of approximation adders is their reduced hardware complexity compared to conventional adders like ripple carry or carry-lookahead adders. This reduced complexity leads to lower power consumption and faster operation. Approximation adders are commonly used in image and video processing applications, where small errors in pixel values may not be visually noticeable. They are also employed in machine learning and neural network accelerators, where approximate results can lead to faster inference while maintaining acceptable accuracy. Ongoing research in approximation adders aims to develop more efficient and accurate approximation techniques. Researchers are working on creating adaptive approximation techniques that can dynamically adjust the level of approximation based on the application's needs and workload. A "single approximation" adder, on the other hand, is designed to provide approximate results for addition operations. It sacrifices some level of accuracy to achieve benefits like reduced power consumption and increased speed. Single approximation consists of Single Exact Single Approximation (SESA) adder and Single Exact Dual Approximation Adder. These are the currently evolving hybrid adders that provide flexible and suitable solutions for developing efficient microprocessors.

The main motto is mentioned as follows,

- To improve speed and resource efficiency
- To improve the efficiency of signal-processing processor chips
- To maintain low-power energy
- To have better efficient real-time application results

The next section (2) describes background work. It is followed by section (3) system model. Section (4) talks about comparison and discussion then section (5) describes the conclusion of the work.

2. Background Work

Using adders in DSP processors and image processing applications can enhance the results and provide low-energy operations. Many researchers implemented several designs of adders and analyzed them for different VLSI applications. S.E. Fatemieh et al., [3] demonstrated imply-based approximate full adders and get compared them with exact adders for energy consumption. The

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Page No: 19 - 23
https://irjaeh.com

PSNR value of this scheme is 80%. X. Jin et al., [4] proposed an 8-bit non-volatile full adder with the method of magnetic tunnel junction for image processing application of gaussian filter. A. Sadeghi et al., [5] implemented an approximation computing technique with the help of a full adder with 12 transistors and ripple carry adder for many image processing applications but does not mention low-power energy techniques. To overcome this Gulafshan et al., in [6] formed a circuit based on 45nm CMOS technology with full adders. In this scheme, full adders primarily use SRAM-based sense amplifiers and it is used to smooth images in image processing applications. J. Lee et al., [7] proposed an approximate adder with truncation methods and decreased error distance with improvised mean values. This scheme is used in applications of machine learning, Digital Image Processing (DIP). Furthermore, it reduces the error rate by 75%. A. Amirany et al., [8] 8-bit approximation adder with MTJ techniques. It is mainly used in Gaussian filter applications and offers well-defined performance along with power improvements. In [9] S. Salavati et al. established a full adder with MTJ mechanism for approximation computing in image processing applications. P. Balasubramanian et al., in [10] describe an approximation adder that was implemented using a 28 nm CMOS cell library and demonstrated practical applications of HOAANED for different applications of digital image processing. C.S. Manikandababu et al., [11] proposed a low-power adder and fed it up into the Sobel edge detection and the whole electronic circuit embedded into FPGA. This scheme gives low power and cost-efficient circuit design. W. Liu et al [12] implemented a circuit of approximation adder with a majority logic mechanism. Several case studies are taken in this scheme for error metrics but did not mention the performance and low power energy of the circuit. For this problem, T. Nomani et al., [13] developed an approximation adder for High Definition (HD) and aerial image processing methods. These circuits get simulated and fed up into FPGA LUT architecture. This scheme is also involved in DCT applications and provides a low power consumption rate. This scheme has a faster delay rate of 27.6% than ACA approximation adders. R. Rajaei et al., [14] implemented full adders with a spintronic mechanism and simulated for Gaussian filter designs. It consists of 50% energy efficiency when compared to other schemes and the error distance consists of 2. A. Sinha Roy et al., [15] created an approximation of Least Significant Bit (LSB) adders analyzed error metrics, and compared it with 216 samples of Monte Carlo simulation. Though these schemes offer better error metrics, in several schemes low power metrics and real-time image processing applications are not mentioned. Hybrid approximation adders known as SESA and SEDA adders offer different efficient parameters. These are currently evolving adders and are used sufficiently in next-generation processors.

3. System Model

3.1 Xilinx ISE

Xilinx ISE was primarily used for designing and implementing electronic circuits by digital programming. Many hardware devices can be programmed to perform a wide range of digital logic functions using Xilinx. Xilinx ISE offered a comprehensive set of tools and features for circuit development including Hardware Description Language (HDL) synthesis support for languages like Very high-speed integrated circuit Hardware Description Language (VHDL) and Verilog. Integrated design entry and simulation tools. Along with FPGA placement and routing tools. Additionally, bitstream generation for configuring FPGAs and debugging and verification tools. Xilinx ISE had different versions released over the years with each version offering improvements, bug fixes, and support for newer FPGA devices.

4. Comparison and Discussion

In this section, approximate adders such as ERCPAA, ETAI, HOAANED, SESA, and SEDA are compared and discussed. The main parameters of adders include area, delay, and power. These parameters are mentioned in the table (1) below,

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Page No: 19 - 23
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Adder Design	*Area* (μm^2)	*Delay* (ps)	*Power* (μw)
ERCPAA	128.2	942	35.6
ETAI	108	109	26.3
HOAANED	461.7	105	73.9
SESA	7.9	58.1	0.73
SEDA	12.5	38.4	0.63

Table 1: Parameters of different adder designs

These parameters are analyzed and given in the form of a graphical representation; the given figure (1,2 and 3) shows that the delay of ERCPAA is much greater than the SESA and SEDA adders. Compared to SESA and SEDA adders, the area and power of HOAANED are greater. The overall performance of SESA and SEDA is much better than other approximation adders as described in the graphical representation.

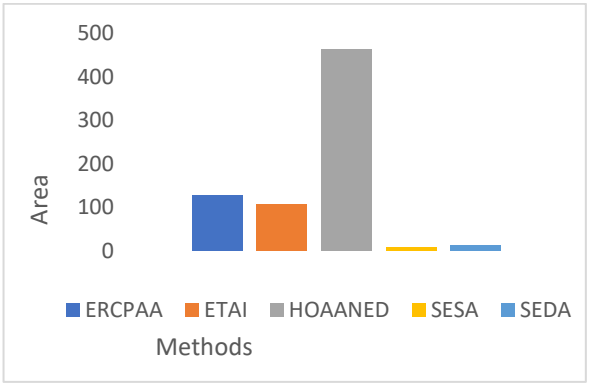

Fig 1: Area of various approximation adders

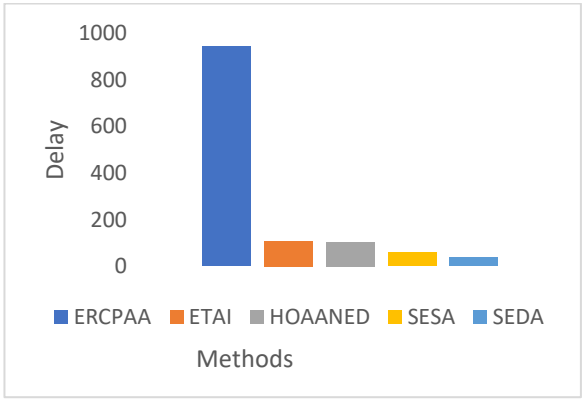

Fig 2: Delay of various approximation adders

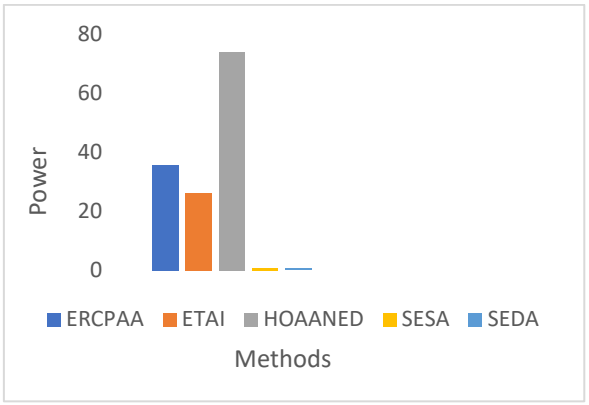

Fig 3: Power of various approximation adders

5. Conclusion

In this work, we presented the survey of approximation adders. Parameters such as area, delay, and power are analyzed and it is discussed. The approximation adders are mainly used in machine learning accumulators and digital image processing. In this survey, when compared to all various kinds of approximation adders, efficient and well-performing adders are given in the form of pictorial representation. These approximate adders use CMOS technology for a greater number of applications. Overall, the highest area and power consumption is given by HOAANED which is 461.7. Moreover, the power consumption is increased with ERCPAA and is given as 942. The major delay consists of 73.9 with a HOAANED adder design. These conditions can tackled by SESA and SEDA adders and further improvements will be made in future schemes. With the help of this survey model, the development and production of efficient approximate adders will be increased and pave the way for choosing correct approximation adders for future-generation microprocessors.

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