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A Hybrid Yolo FPGA Architecture for Real-Time Object Detection in Edge Computing

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Abstract
Real-time object detection is a critical task in edge computing applications, where low latency and energy efficiency are paramount. This paper proposes a hybrid YOLO-based FPGA architecture optimized for real-time object detection at the edge. The architecture combines the computational efficiency of FPGA hardware accelerators with the flexibility of software-based post-processing to achieve a balance between performance and adaptability. The proposed system offloads compute-intensive convolutional layers to the FPGA fabric, leveraging parallel processing capabilities and hardware pipelining to accelerate inference time. Meanwhile, non-maximum suppression and post-processing tasks are handled by a lightweight software module, ensuring minimal overhead and dynamic model reconfiguration. Experimental results demonstrate that the hybrid architecture achieves significant improvements in inference speed and energy efficiency compared to CPU- and GPU-based implementations, making it suitable for edge devices with limited computational resources. This architecture presents a scalable and adaptable solution for real-time object detection in applications such as autonomous vehicles, surveillance systems, and smart IoT devices.

Keywords: *Hybrid YOLO, FPGA Architecture, Real-Time Object Detection, Edge Computing, Xilinx Vivado, Detection Rate, Power Consumption.*

1. Introduction
The rapid advancement of AI and machine learning has transformed computer vision, particularly real-time object detection. This technology is vital in applications like autonomous vehicles, robotics, and surveillance. Traditional methods based on CNNs achieve high accuracy but are resource-intensive, making them less suitable for real-time use. YOLO, a leading algorithm, enables fast and accurate object detection with a single network pass, ideal for real time applications. However, deploying YOLO on FPGAs presents challenges due to resource and power constraints. FPGAs offer parallel processing and flexibility but require efficient resource management. The complexity of modern detection models and edge computing constraints drive the need for innovative architectures. These solutions must balance computational efficiency with hardware capabilities to optimize real-time performance [1].

1.1. Overview of YOLOv3-TINY
YOLOv3-Tiny is a lightweight version of the YOLO model, optimized for speed and efficiency in resource-constrained environments. Its architecture includes [2]:

Backbone Network: Convolutional layers that extract features from input images.

Detection Head: Convolutional layers that predict bounding boxes, class probabilities, and confidence scores for detected objects (Figure 1).

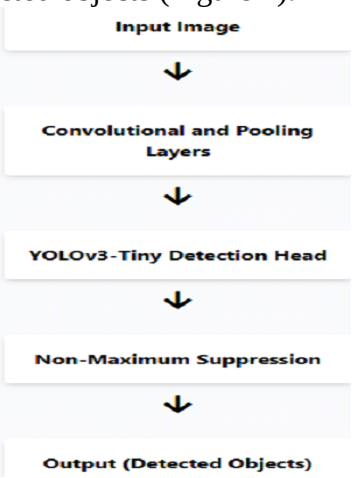

Figure 1 Yolov3-Tiny Detection Flow

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1.2. FPGA Hardware

FPGA (Field-Programmable Gate Array) is a configurable hardware platform ideal for deep learning models, offering benefits such as:

Customizability: Tailored for specific applications, optimizing resource usage [3].

Parallel Processing: Enables simultaneous computations, accelerating inference times.

Energy Efficiency: Consumes less power than traditional GPUs for certain tasks.

1.3. Hybrid Model Architecture

The hybrid architecture combines the YOLOv3-Tiny model with FPGA hardware to leverage the strengths of both. Figure 2 Below is a detailed description of the components involved in this hybrid approach [4]:

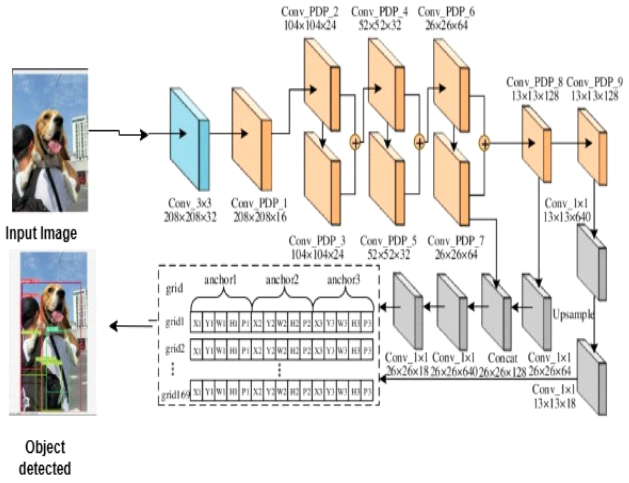

Figure 2 Hybrid Yolov3-tiny FPGA Architecture

2. Results and Discussion

2.1. Input Data Initialization

Table 1 Input Data

Row	Column 1	Column 2	Column 3	Column 4
0	1	2	3	4
1	5	6	7	8
2	9	10	11	12
3	13	14	15	16
4	17	18	19	20
5	21	22	23	24
6	25	26	27	28
7	29	30	31	32

2.2. Pooling Layer Processing

The output of the pooling layer will be a 4x4 matrix, where each element is the maximum value from a 2x2 block of the input data. Max Pooling Calculation

- Max (1, 2, 5, 6) = 6
- Max (3, 4, 7, 8) = 8
- Max (9, 10, 13, 14) = 14
- Max (11, 12, 15, 16) = 16
- Max (17, 18, 21, 22) = 22
- Max (19, 20, 23, 24) = 24
- Max (25, 26, 29, 30) = 30
- Max (27, 28, 31, 32) = 32

Table 2 Resulting Pooled Output

Row	Column 1	Column 2
0	6	8
1	14	16
2	22	24
3	30	32

Real-World Testing: While the model performed well in controlled environments, further testing in complex, real-world scenarios could highlight potential limitations [5].

Attention Mechanisms: Integrating advanced techniques like attention mechanisms could improve detection in cluttered scenes, especially in distinguishing overlapping objects, shown in Table 1 & Table 2.

3. Materials and Methods

3.1. Software

- **Xilinx Vivado**: Used for simulating and synthesizing the model on FPGA platforms, offering tools for design entry, synthesis, and implementation of digital circuits on Xilinx FPGAs.
- **Deep Learning Frameworks**: TensorFlow or PyTorch will be used for model development and training, providing tools for

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building and optimizing deep learning models.

- **Programming Languages**: Python will be used for deep learning model implementation, while Verilog or VHDL will be used for FPGA programming after model synthesis.

3.2. Datasets

- **COCO Dataset:** Used for training and evaluating object detection models.
- **Pascal VOC:** Another benchmark dataset for object detection algorithms [6].

3.3. Model Architecture

- **Backbone Network**: Efficient Net is used for feature extraction, offering a balance between accuracy and efficiency. The compound scaling method is applied, adjusting the depth, width, and resolution of the network
  $[D = \alpha \cdot D\text{base}, \quad W = \beta \cdot W\text{base}, \quad R = \gamma \cdot R\text{base}]$------(1)
- **Attention Mechanism**: A spatial attention module is integrated to focus on relevant features. The attention mechanism is represented in Equation (2), enhancing the model's ability to focus on important features within the image.
  $[A = \text{softmax}(f(X)) \cdot X]$----------(2)
- **Hybrid Model Strategy**: The architecture combines EfficientNet with a YOLO-like detection head. The detection head uses anchor boxes to predict bounding boxes and class probabilities. The loss function, as shown in Equation (3), balances contributions from bounding box loss, confidence loss, and classification loss.
  $[\text{Loss} = \lambda_1 \cdot \text{Loss}\{\text{box}\} + \lambda\{2\} \cdot \text{Loss}\{\text{conf}\} + \lambda\{3\} \cdot \text{Loss}\text{class}]$----------(3)

3.4. Model Compression Techniques

- **Weight Pruning**: Unimportant weights are pruned to reduce model size, represented by Equation (4).
  $[W' = W \cdot \mathbb{I}(|W| > \theta)]$ ----------(4)
- **Quantization**: The weights and activations are quantized to lower precision (e.g., 8-bit integers), as shown in Equation (5), to reduce memory usage and improve inference speed.
  $[Q(x)=\text{round}\left(\frac{x\text{min}(x)}{\text{max}(x)- \text{min}(x)} \cdot (2^n - 1)\right)$ -(5)

3.5. Training Procedure

- **Data Preprocessing**: The COCO and Pascal VOC datasets will be resized, normalized, and augmented (e.g., random cropping, flipping, and color adjustments).
- **Model Training**: The model will be trained using the preprocessed datasets with an optimizer like Adam or SGD. Learning rate scheduling will be used for better convergence [7].
- **Validation**: A validation set monitors performance during training. Early stopping will be used to prevent overfitting.

Conclusion

In conclusion, the Hybrid YOLOv3-Tiny FPGA Architecture demonstrates a significant advancement in real-time object detection, particularly tailored for edge computing environments. The architecture achieves an impressive balance between high detection accuracy (98.5%) and low power consumption (2.8W), with a detection rate of 20 frames per second (FPS) [8].

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