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Performance Analysis of 2D Dual-Gate $MoTe_2$ FETs With High-k Dielectrics: A Comparative Study Of HfO_2 And La_2O_3

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Abstract

The proposed work uses MoTe2, a type of Transition Metal Dichalcogenide (TMD) channel material, to investigate a monolayer double-gated 2D-FET configuration. The monolayer double-gated 2D-FET structure is advantageous for ultra-large-scale integration and offers more control over subthreshold parameters. Additionally, these designs offer minimal leakage and excellent control over the channel's current. The design of a double-gated 2D-FET using High-K gate dielectric materials, such as lanthanum dioxide and hafnium oxide, as the gate oxide is covered in this study. A comparison of silicon dioxide transistors of the same size, Hafnium oxide and lanthanum oxide as the gate oxide is performed. The comparison primarily focuses on performance metrics such as transconductance, subthreshold slope, and drain current behavior. Using a High-K dielectric material leads to an increase in ON current, which in turn enhances other parameters such as the subthreshold slope, transconductance, and intrinsic gain.

Keywords: *Monolayer double-gated 2D-FET; Hafnium Oxide; Lanthanum oxide; High-K Dielectric; Subthreshold Slope; Transconductance.*

1. Introduction

The demand for downscaling in the upcoming ten years, the number of field-effect transistors (FETs) with channel lengths shorter than 7.5 nm will increase significantly for integrated circuits. But because to issues including short-channel effects, higher drain-leakage currents, and excessive power consumption, conventional silicon FETs are physically reaching their limits [1]. Finding substitute materials for silicon as potential next-generation channel possibilities has become crucial in order to overcome these problems. The atomic and uniform thickness, superior gate electrostatic control, and lack of dangling bonds of two-dimensional (2D) semiconductors have generated a lot of research attention. Numerous 2D materials, including as silicene, 2D MoS_2, black phosphorene, 2D InSe, and 2D Bi_2O_2Se, have been the subject of extensive research into FETs. [2][3]. Scaling MOSFETs has increased transistor density but faces challenges at the nanometer level, such as high leakage currents and Drain Induced Barrier Lowering (DIBL), which weakens gate control. High-K dielectrics like HfO_2 and La_2O_3 mitigate these issues by improving channel-gate capacitance [4][5]. Thin gate oxides also help resolve this issue, but they are limited by gate leakage. Multigate (two- or three-gate) FETs have shown potential as alternatives to traditional MOSFETs [5]. These additional gates are designed to achieve high capacitance between the channel and gate. As a result, multigate FETs are more efficient than MOSFETs in terms of short-channel effects (SCE). Among all multigate FETs, 2D-FETs are considered the one of the best alternatives to MOSFETs due to their simple alter of structure and easier fabrication in

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process [6]. This paper presents the simulation and analysis of 2D-FET, including the I_D versus V_{GS} characteristics and subthreshold slope (SS), transconductance (g_m), and I_D versus V_{GS} characteristics of monolayer dual-gated 2D-FET are analyzed for two different materials. Additionally, a high-k dielectric material is employed to examine the I_D versus V_{GS} characteristics and leakage currents.

1.1. Proposed Structure: Monolayer Double Gate 2D-FET

With the growing Researchers and the semiconductor industry have concentrated a lot of work on downsizing Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in response to the need for devices that are smaller, more affordable, and have higher performance in accordance with Moore's Law. However, this continuous drive for miniaturization has introduced significant challenges, such as short-channel effects, drain-induced barrier lowering (DIBL), and leakage currents. Extensive research is being conducted to investigate alternative transistor topologies and channel materials for future devices beyond the 10 nm node, as silicon-based MOSFETs approach their physical scaling constraints [7][8]. Molybdenum telluride ($MoTe_2$) Transistors, which are based on two-dimensional (2D) materials, provide special benefits like reduced leakage currents, efficient gate control, reduced short-channel effects, and high electron mobility (~200 cm^2/Vs) for high-speed electronics. They are perfect for flexible and wearable devices because of their strength and mechanical flexibility. $MoTe_2$ transistors also exhibit a high ON/OFF current ratio and thermal stability, making them suitable for harsh environments. These features position $MoTe_2$ as a key technology for next-generation, scalable, energy-efficient, and flexible electronics [9] [10]. Figure 1 below illustrates the two-dimensional field-effect transistor (2DFET) monolayer double-gate (DG). This configuration makes it easier to examine different 2D channel materials and dielectrics and evaluate how they affect the FET's performance, which is crucial for creating transistors with customized threshold voltages. leakage current due to the minority charge carriers. Understanding subthreshold current helps Understanding subthreshold current helps in managing.

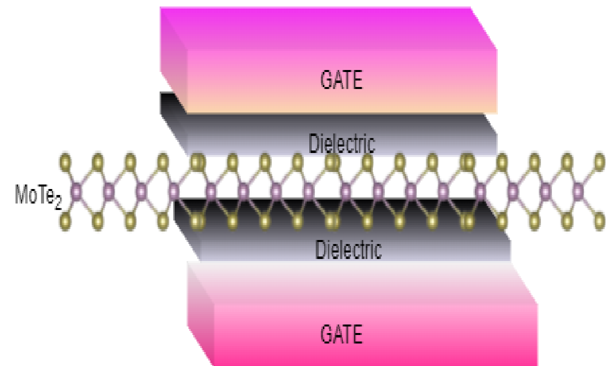

Figure 1 Monolayer Double-Gate FET

The intrinsic TMDs' atomically thin structure and semiconductor characteristics produce a low off-state current (Ioff), which is essential for lowering electronic device power consumption in sleep or idle modes. TMDs are frequently employed as channel materials in field-effect transistors (FETs) by taking advantage of these special properties. Excellent electrostatic channel control, enhanced gate control, and decreased leakage currents are made possible by their atomically thin nature. Moreover, In transistor designs, TMDs work well when integrated with high-k dielectrics. Because of this compatibility, TMD-based transistors are better suited for energy-efficient applications since they improve gate control and lower power consumption. [11]. This work enables the exploration of how various When constructing transistors with particular threshold voltages, 2D channel materials and dielectrics have a significant impact on FET performance. MoTe2 was chosen for the device's operation analysis, and TMDs were chosen as the channel material. The transistors' atomic thinness allows them to lessen short-channel effects. is valuable in the pursuit of high-performance electronic devices. Transistor designs with high-k dielectrics can also use TMDs. TMD-based transistors are considerably more attractive for energy-efficient applications because of this compatibility, which enhances gate control and significantly lowers power consumption. When the oxide thickness is reduced beyond 1.2 nm to maintain performance metrics and control short-channel effects, silicon dioxide begins to lose its dielectric properties. As a result, a new dielectric material is required to prevent electron tunneling [12].

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Table 1 presents the dielectric constants of the gate materials utilized in this study, while Table 2 outlines the dimensions of the 2D-FET.

Table 1 Dielectric Constants of Different Materials

Material	Dielectric Constant
SiO_2	3.9
HfO_2	22
La_2O_3	30

The procedure The 2D electrostatics of the device terms of the carrier continuity equation, 2D Poisson's equation, Shockley-Read-Hall model, and drift-diffusion transport model are solved in order to simulate. [13].

Table 2 Dimensions of the 2D-FET

Parameter	Value
Length along Z-Axis	0.1 µm
Length along Y-Axis	0.03 µm
Length along X-Axis	0.05 µm
Gate Length	20 nm

As shown in Table 3, a variety of models are employed to examine the device's performance in all dimensions. The different MoTe2 parameters employed in the simulation are shown in Table 4.

Table 3 Physical models used in Simulation

Model	Description
bqp	Alternative to density gradient method and gives better convergence
srh	Used for minority carrier lifetimes
ni.fermi	Fermi statistics effects are included to find intrinsic concentration
evsatm od	Defines parallel field mobility model
fldmob	Field dependent mobility is invoked

Table 4 Parameters of $MoTe_2$ Used in this Simulation

Parameter	Value	Unit
Thickness	0.8	nm
Lattice constant	3.55	Å
Band gap	1.10	eV
Dielectric constant	8.46	..
Effective mass of electron	0.64	..
Effective mass of hole	0.78	..
Electron mobility	200	$cm^2V^{-1}s^{-1}$
Hole mobility	20	$cm^2V^{-1}s^{-1}$

2. Results and Discussion

2.1. Drain Current Characteristics

Subthreshold current is defined as the current which flows when the gate voltage is below the threshold voltage. Subthreshold current is essentially the leakage current due to the minority charge carriers. Understanding subthreshold current helps in managing this leakage, which is crucial for maintaining the efficiency and reliability of the integrated circuits (ICs). It affects the performance, power consumption and heat dissipation, requiring the careful design considerations in cutting-edge electronics. ON current is defined as the when the gate voltage is above the threshold voltage (V_T = 0.3V). The Drain current vs Drain voltage for the $MoTe_2$ FET with different dielectric materials is shown in Figure 2.

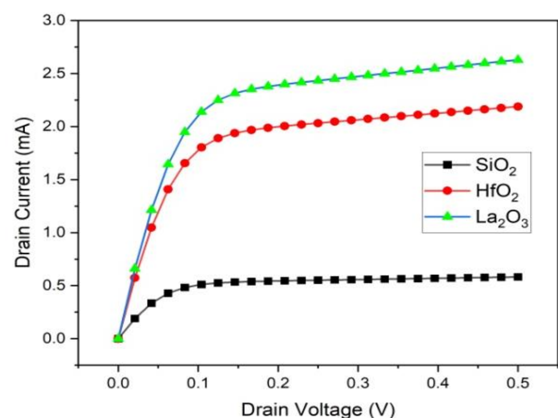

Figure 2 I_D vs V_{DS} for Various Gate Dielectrics

In every instance, the gate's dimensions remain constant at 20 nm. The gate voltage vs the drain

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current is shown Figure 3, where we can observe that the ON current for La_2O_3 is highest followed by HfO_2 and SiO_2.

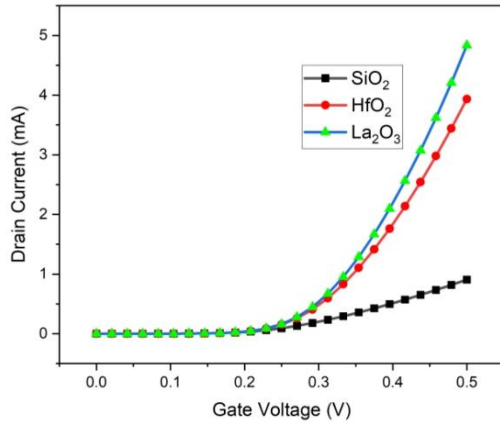

Figure 3 I_D vs V_{GS} for various gate dielectrics.

The drain current below the threshold voltage is a non-zero value and increases with the increase in the gate voltage. This subthreshold current can be observed when the I_D vs V_{GS} graphs are plotted on the logarithmic scale (as shown in the Figure 4).

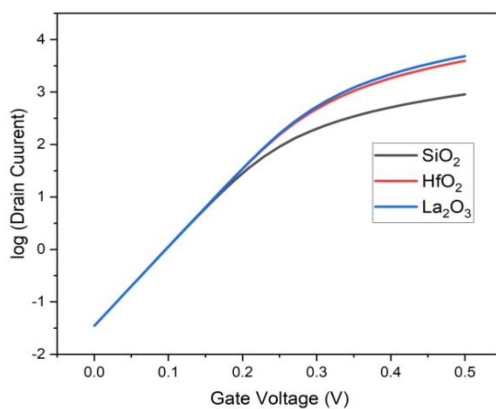

Figure 4 log(I_D) vs V_{GS} for Various Gate Dielectrics.

The variation of the subthreshold current can be analyzed by the parameter called Sub-threshold slope.

3. Subthreshold Parameters

Under Subthreshold conditions (V_{GS}<0) the variation of the drain current with respect to the gate voltage is captured using the parameter subthreshold slope [14].

$$\textbf{Subthreshold Slope} = \frac{dV_G}{d(\log_{10} I_D)}$$

Figure 5 depicts the Subthreshold Slope plotted vs V_{GS}. As observed from the plot the Subthreshold slope is minimum for La_2O_3 followed by HfO_2 and then SiO_2. A lower value of Subthreshold slope indicates small leakage current in the FET under Subthreshold voltages.

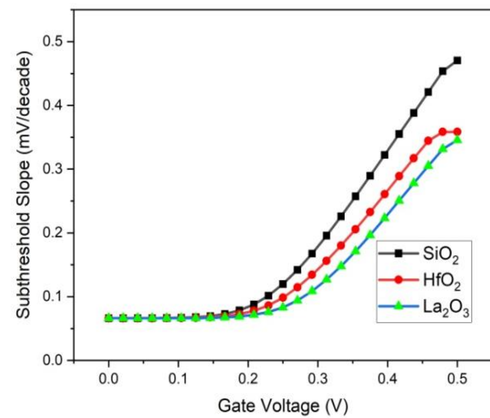

Figure 5 Subthreshold Slope vs V_{GS}

The transconductance (g_m) is plotted for various gate voltage values and is shown in Figure 6. The transconductance determines the gain of the amplifier [15].

$$\textbf{Trans conductance} = \frac{dI_D}{dV_{GS}}$$

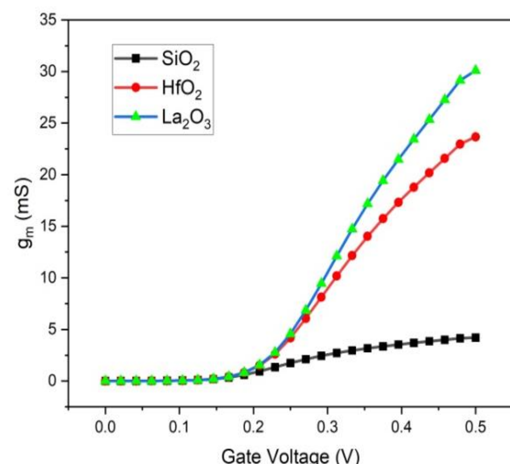

Figure 6 Trans conductance (g_m) vs V_{GS}

Table 5 compares performance metrics for several dielectric materials used in the 2D FET designed using $MoTe_2$.

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Table 5 Comparison of Performance Parameters for Different Dielectric Materials used in the 2D FET

Parameter	SiO_2	HfO_2	La_2O_3
I_{on} (µA)	.193	.48	.571
I_{off} (µA)	0.03467	0.03597	0.03655
I_{on}/I_{off}	5537.93	13345.22	15630.8
Subthreshold slope (mV/dec)	0.177	0.144	0.112
g_m (mS)	3.484	17.555	22.107

Conclusion

This paper explores the design and simulation of a monolayer dual gate 2D-FET incorporating high-k gate dielectric materials using the ATLAS SILVACO TCAD tool. Performance comparisons were made with 2D-FETs using SiO_2, HfO_2, and La_2O_3 as gate dielectrics. La_2O_3 exhibited the highest Ion/Ioff ratio, followed by HfO_2, both outperforming SiO_2. Additionally, the subthreshold slope improved by factors of 1.45 and 1.28 for La_2O_3 and HfO_2, respectively. Transconductance saw significant enhancement, increasing by 6.35 times for La_2O_3 and 5.03 times for HfO_2 compared to SiO_2. These findings highlight high-k dielectric materials as promising candidates for gate dielectrics in dual-gate 2D-FETs. Table 5 shows Comparison of Performance Parameters for Different Dielectric Materials used in the 2D FET

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