International Research Journal on Advanced Engineering Hub (IRJAEH)
e ISSN: 2584-2137
Vol. 02 Issue: 11 November 2024
Page No: 2581 - 2585
https://irjaeh.com
https://doi.org/10.47392/IRJAEH.2024.0355

Area-Efficient Gray Code Counter Design Using Hybrid Flip-Flop

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Abstract

Chip area plays an important part in the advancement of semiconductor technology, enabling integrated circuits to get smaller and smaller over time. Numerous advantages result from this reduction, including higher production yield, better energy efficiency, better system performance, and lower component density in packaging. We are Utilizing [2] 18-transistors hybrid flip-flop structure to design a Gray code counter (GCC) [2] with asynchronous clock input, the design is useful for high-performance implementations, Gray code is a unit-distance coding technique that significantly decreases error propagation in communication networks by altering only one bit every transition. The suggested design outperforms traditional Gray code counters by reducing the area by about 30.49%. The implementation operates in the voltage range of 0.7-1.2V and has a transient response time of 300ns. Cadence Virtuoso in 45nm is used to accomplish it.

Keywords: *Gray code counter, Area optimization, hybrid flipflop, clock gating.*

1. Introduction

A counter is a digital circuit that sequences bits based on the type of counter chosen for the specific application. Its output depends on both the current input and previous outputs. According to [9], Mirrored Binary, Maximum Space, Equilibrated, Perpendicular, and Non-Composite Gray Codes are examples of different variations of gray codes. A synchronous counters and synchronous counters are the two main types of counters. Synchronous counters guarantee that every stage of the counter changes states concurrently by applying a common clock signal to every flip-flop simultaneously. While asynchronous counters, depending on the bit size of the counter, apply the clock signal to the initial flipflop and use its output to drive the subsequent flipflop in the sequence, as opposed to applying the clock signal input simultaneously. The counter setup is simplified since the asynchronous clock input eliminates the need for intricate clock delivery methods. In order to create a standard counter for comparison, a positive edge-triggered D flipflop is used in the gray code counter design . Conversely, the design of another employs an 18T hybrid flip-flop structure. In order to minimize circuit complexity and provide greater performance across a range of supply voltages and operating frequencies, the counter design makes use of a hybrid flip-flop. [1]

2. Related Work

The schematic and simulations of the master-slave architecture in the hybrid flip-flop are presented in Figures 1 and 2, and its operation is as follows. From [2] (Data = 0, Clock = 0): N6 and N7 are inactive, letting the slave keep its previous value; P3, P2, and N4 deliver an assertive 1 and a gentle 0 to the master node, respectively. P1, P2, and N4 activate, causing u1 to become 1. N6 sends a solid 0 to node "a" and a gentle 1 to node "b" when N6 and N7 engage and begin transferring data from the master to the slave (Data = 0, Clock = 1). (Data = 1, Clock = 0): N1, P2, and P4 engage, setting u1 and u2 to 0, and P2 delivers a gentle 0 at u1, while P3 sends a solid 1 at the master node. The head keeps one. (Data = 1, Clock = 1): During the data transfer from the master to the slave, N7 delivers a gentle 1 to node "a" and a solid 0 to node "b". The design Figure 1 Shows that the circuit's supply voltage, VDD, varies between 0.7V and 1.2V. The substrates of the PMOS and NMOS transistors are connected to VDD and ground,

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respectively. Additionally, P3 receives the clock-gated input, and the data signal is positioned between the P1 and N1 transistors. [2,3]

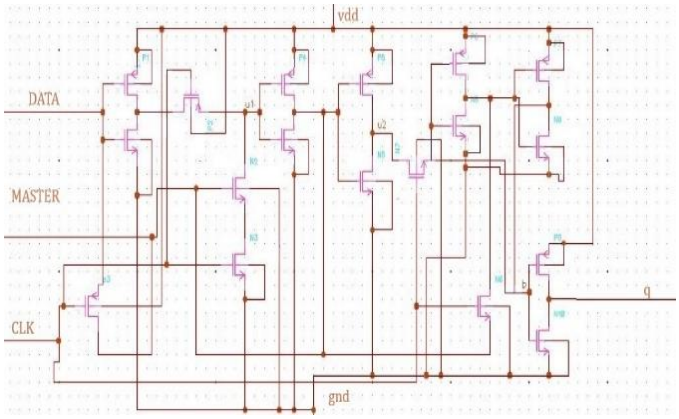

Figure 1 CMOS Arrangement of 18 Transistor Hybrid Flipflop

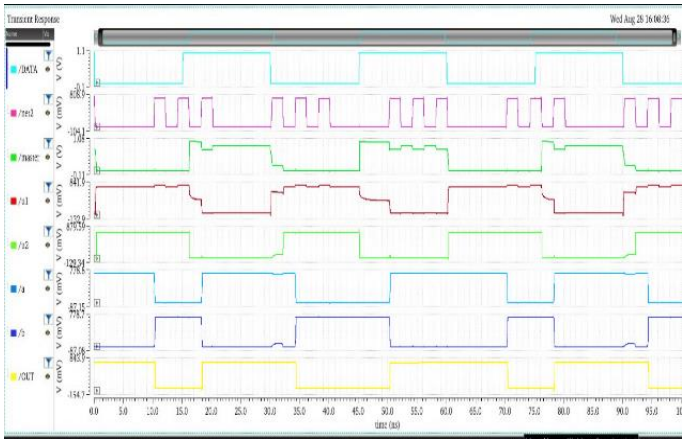

Figure 2 Output Waveforms for The Clock-Gated Hybrid Flipflop

It has four transmission gates (P2, P3, N6, and N7), two pairs of which serve as current enhancers and assistive transistors, respectively. Figure 2 shows that the clock is in power-saving mode, which will cause it to shut off after a predetermined amount of time. Because it's semi-static, it won't stay in one place for too long, and it will choose how long the power-saving phase lasts depending on the input signal sent into the circuit. [5]

3.Proposed Work

Figure 3 outlines the particular stages of the suggested design. The circuit can be simulated to confirm that the MOS transistors are first set up to function as anticipated. Following this, we will create the design layout using the schematic transistor configuration. Later, Design Rule Checking (DRC) is carried out to confirm that every component operates in accordance with the designer's specifications. The last phase is to compare the layout to the schematic drawing using Layout versus Schematic (LVS). Cadence Virtuoso in the 45nm technology node is used to carry out this complete operation. The subsequent state table (Table 1) represents the source binary sequence and derived Gray code sequence for both Gray code counters. [4]

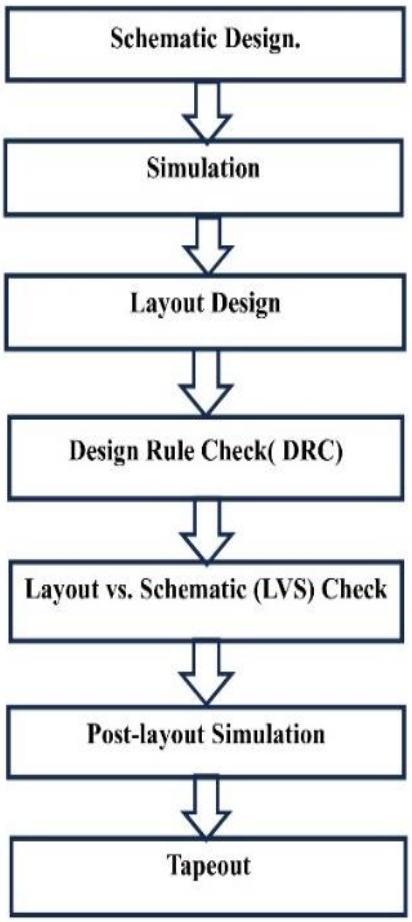

Figure 3 Flow Chart for The Proposed Design Process.

The last phase is to compare the layout to the schematic drawing using Layout versus Schematic (LVS). Cadence Virtuoso in the 45nm technology node is used to carry out this complete operation. The subsequent state table (Table 1) represents the source binary sequence and derived Gray code sequence for

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both Gray code counters. The subsequent state table (Table 1) represents the source binary sequence and derived Gray code sequence for both Gray code counter. [6,7]

Table 1 State Table for Gray Code Counter

Existing State				Subsequent State			
q3	q2	q1	q0	q3	q2	q1	q0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

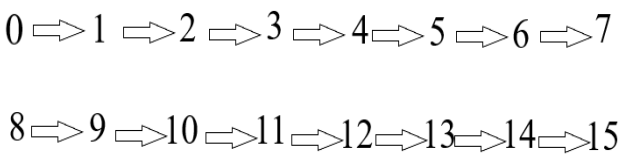

Figure 4 Entry Binary Sequence in Decimal Representation.

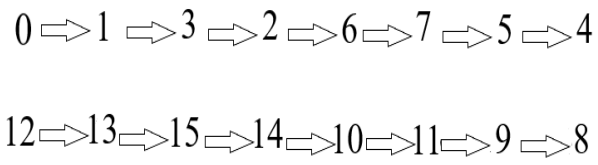

Figure 5 Derived Gray Code Sequence in Decimal Representation.

Table 1 shows the State Table for gray code counter Figure 4 shows the Entry binary sequence in decimal representation. Figure 5 shows the Derived gray code sequence in decimal representation. To avoid racing situations, we are using a positive rather than a D flip-flop, an edge-triggered D flip-flop, which often produces a toggling effect. Only at the clock's positive edge does the output change. To create Gray code counters, XOR gates & Posedge D-flip-flops are both utilized. Figure 6 Shows the Gray code counter using positive edge triggered flipflop. [8]

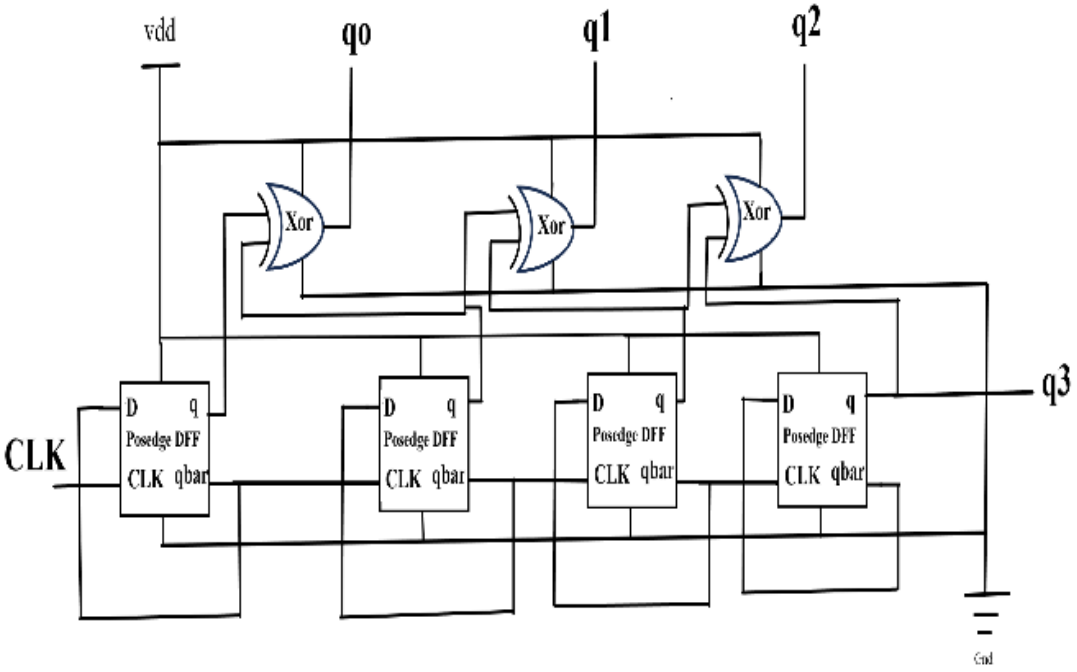

Figure 6 Gray Code Counter Using Positive Edge Triggered Flipflop

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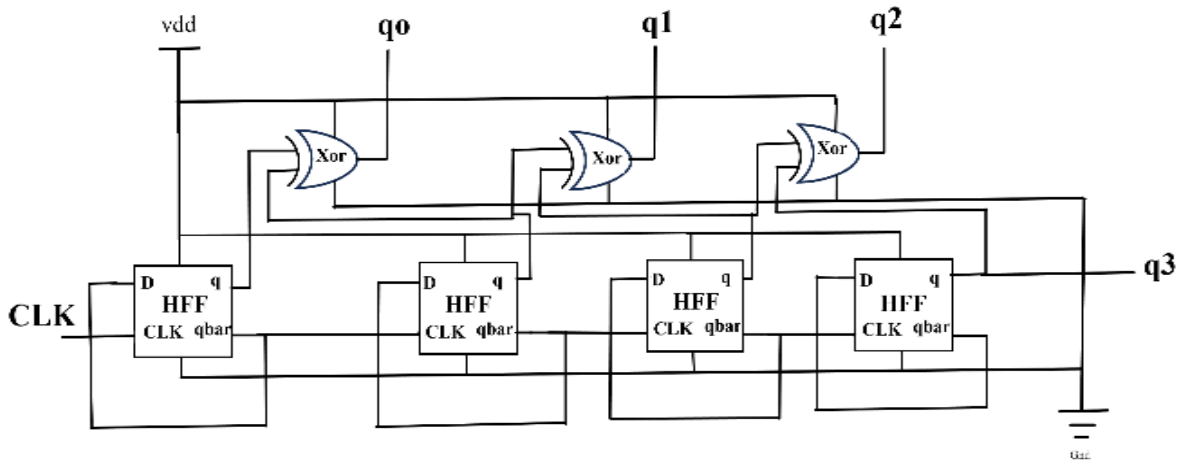

Figure 7 Gray Code Counter Using Hybrid Flipflop

With the exception of using an internal hybrid flip-flop configuration in place of a D flip-flop, this design is identical to the previous concept (Figure 6). In accordance with the serial-in parallel-out (SIPO) paradigm, which uses serial clock as input, outputs are taken across XOR gates synchronously as Q3 Q2 Q1 Q0, where Q3 is the most significant bit (MSB) and Q0 is the least significant bit (LSB). Below are simulations for both counters. Figure 7 shows the Gray code counter using Hybrid Flipflop.

4. Results and Discussion

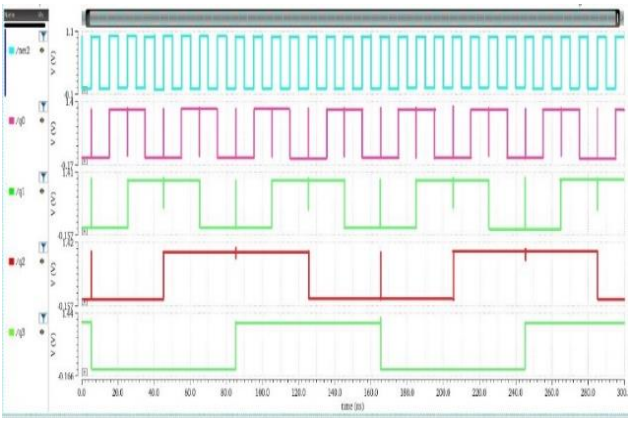

Figure 8 Gray Code Counter Simulations Using Positive Edge Triggered D Flipflop

The outcomes are consistent with the state table given in Table 1 based on Figures 8 and 9 above. Transitions start with q3 and happen at every positive clock edge. The clock changeover is indicated by the line that shows up in the center of the square pulse. Since both are intended to perform the same function, the simulated waveforms are similar, continuing into the 300 ns transient response phase. Table 2 shows Observation of different gray code counter circuits. [10]

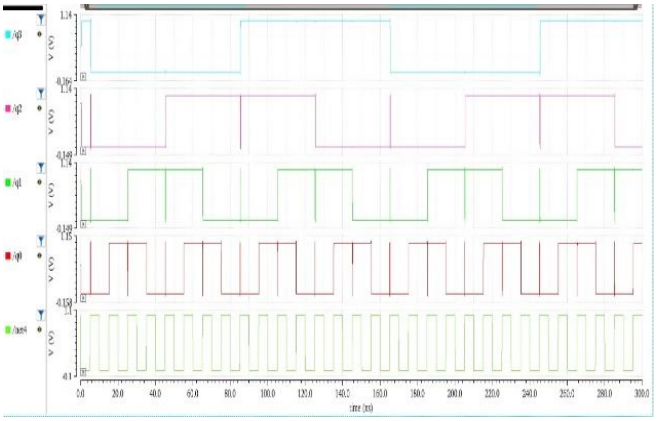

Figure 9 Gray Code Counter Simulations Using Hybrid Flipflop

Table 2 Observation of Different Gray Code Counter Circuits

Parameter	GCC using positive edge triggered DFF	GCC using hybrid FF
Transistor Count	120	96
Layout Area(μm²)	235.9	101.4

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Conclusion

In summary, we have achieved a lower transistor count in our hybrid flip-flop gray code counter concept, which can consequently reduce the layout area of the design. Our suggested method has reduced the area by about 30.49% when compared to the conventional gray code counter design. It is particularly ideal for high-performance applications because the hybrid flip-flop's shape uses fewer PMOS transistors and clock overloading has been reduced.

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