

Analyzing Work Function Dependency for Doping Variations in Double Gate Junction Less Field Effect Transistor: A TCAD Simulation Perception

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Abstract

In this investigation, we present effect of work function on variation of electrical performance of conventional Double Gate Junctionless Field Effect Transistor (DGJLFET) for various range of doping profiles. By using TCAD simulator, the impact of doping concentrations spanning from 10¹⁰ cm⁻³ to 10¹⁹ cm⁻³ and work functions of 5.0 eV, 5.2 eV, and 5.4 eV is comprehensively explored. In this work the electrical parameters including threshold voltage, On Current, Off Current, On Current to Off Current ratio, and Subthreshold Swings are analyzed for each work function setting. Results indicate an interrelationship between higher doping levels and increased On Current, alongside a reduction in Subthreshold Swing. Notably, at a work function of 5.4 eV and a doping concentration of 10¹⁹ cm⁻³ threshold voltage obtained is 0.71 V, I_{ON}/I_{OFF} is 3.75 and Subthreshold Swing is 75 mV/decade are accomplished demonstrating the potential for optimized transistor performance through work function engineering.

Keywords: Doping profile; Junctionless Field Effect Transistor; On Current; Subthreshold swing; Threshold Voltage.

1. Introduction

Recently challenges have been made for fast scaling down of MOSFET. In order to continue with Moore's law, various devices of semiconductor have been suggested till date including nano structured devices such as quantum devices and high electron mobility devices. Also the size of MOSFET are reduced continuously in order to enhance the performance and low power consumption and thereby later on SCE (Short Channel Effect) are developed. Moreover various challenges have been confronted by lessening the size of the device thereby causing Short Channel Effects (SCE) such as drain induced barrier lowering (DIBL), channel length modulation, surface scattering, etc. In order to curtail all these SCE multigate MOSFETS were introduced [1-17]. However in order to overcome the challenges faced by SCE researchers have developed the proposal of Junction free transistor having uniform doping with no doping concentration gradients. The fabrication process and production cost of JLFET is less compared to Metal oxide FET [18]. Therefore, JLFETs seems to be a encouraging substitute to the standard MOSFETs [19]. Both the source and drain region proceeds towards each other to decrease the multigate MOSFET gate. Subsequently the channel is predominated by source, drain and gate which results in various SCEs in multigate MOSFET. Later on in order to overcome this difficulty, researchers proposed a new device naming Junctionless FET (JLFET). The foremost fabrication of JLFET was done by Collinge et. al. in the year 2009 [20]. Here source, channel and drains has a constant doping level. Mostly the silicon Junctionless nanowire transistor (JNT) is observed and considered to be one of the most favourable alternatives for future integrated circuits and has gained utter attention due to its



simple and easy fabrication process, extremely low short channel effects, near ideal subthreshold slope and having outstanding gate control ability [21-25].Moreover for scaling, low process flow and t has become most interesting semiconductor device. Therefore this VLSI design Junctionless Field Effect Transistors (JLFET) is gaining popularity in the field of VLSI design because of its various benefits over conventional MOSFET such as superior Ion/Ioff ratio, fast switching time, low power consumption, and excellent controllability of gate over the channel potential.One among them is the high off state current, carrier mobility degradation resulting from high doping concentration. It also has some major drawbacks which can be mitigated by the usage of a thin channel. With greater doping concentration the drain current produced will be larger, however the drawback is larger subthreshold slope which is also achieved due to wider channel preventing fulldepletion. But a thin channel will lower the on current creating the channel resistance to be high. Therefore JLFET can reduce SCE provided there is a very high doping profile in the substrate segment causing degradation in carrier mobility. The various conditions are necessary for turning the device off such as- a high work function variance between the channel and the gate region which also predominant in turning off the device. The device turn on current of JLFET is very high as the substrate is heavily doped. In this work a simulation method has been performed considering doping variation in DGJLFET based on different work functions. The study focuses on elucidating how variations in the work function impact on the performance of Double Junctionless Gate Field Effect Transistors (DGJLFET). Moreover, the study seeks to identify relationship between work function, doping concentration, and transistor performance metrics, providing insights into the underlying mechanisms governing DGJLFET behavior. Additionally, by pinpointing optimal combinations of work function and doping profile, the research aims to highlight strategies for enhancing the electrical performance of DGJLFETs, potentially paving the track for enhanced transistor designs in future semiconductor technologies.

2. Structure and Simulation Setup

For simulation analysis a N-channel Double Gate Junctionless Field Effect Transistor has been considered. Figure.1 demonstrates the structural diagram of DGJLFET. The length of source and drain are considered as $L_s = L_d = 10$ nm. In addition, the gate length (L_g) of device is considered as 10 nm. So, total size of the device is 30 nm. The thickness (t_{si}) of the body of the device is 10 nm. The oxide thickness (t_{ox}) is considered as 3 nm and gate thickness is 2nm. Work functions are considered as 5.0 eV, 5.2 eV and 5.4 eV. In this structure the doping is varied from 10^{10} cm⁻³ to 10^{19} cm⁻³. For performing the simulation of various electrical parameters COGENDA Visual TCAD simulator is used considering Band to Band tunnelling for all simulations.

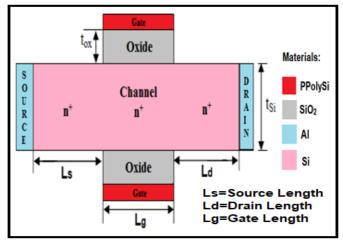


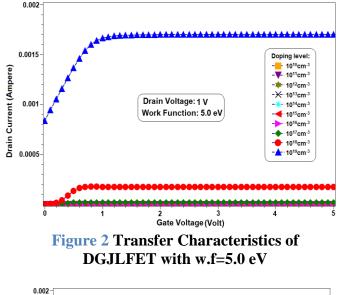
Figure 1 Schematic Diagram of DGJLFET

3. Results And Discussions

The transfer characteristics of doped DGJLFET for work functions 5.0 eV, 5.2 eV and 5.4 eV are presented in Figure 2, Figure 3 and Figure 4 respectively. From the above figures it can be observed that the drain current is maximum for doping at 10^{19} cm⁻³ for all the work functions. The On current is maximum at a value of 0.00168A for work function 5.0 eV, 0.001698 A for work function 5.2 eV and 0.00171 A for work function of 5.4 eV at a doping level of 10^{19} cm⁻³. It has been observed that with higher work function ON current value is also high.



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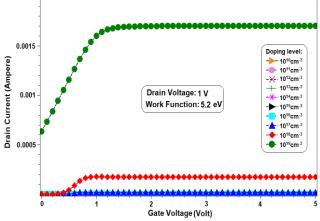
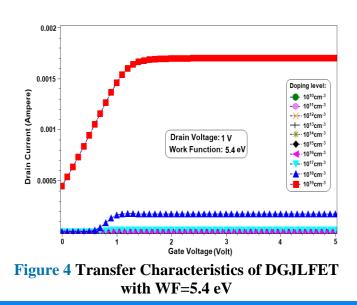


Figure 3 Transfer Characteristics of DGJLFET with WF=5.2 eV



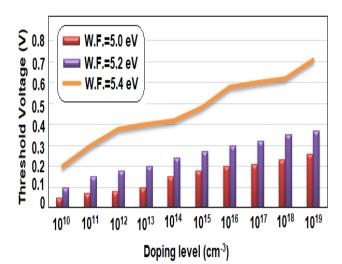


Figure 5 Threshold Voltage vs. Doping Level for Different Work Functions

From Figure 5 it can be analysed that the value of threshold voltage increases with an increase in work function value for different doping variation from 10^{10} cm⁻³ up to 10^{19} cm⁻³. However, at work function 5.0 eV threshold voltage increases gradually with increases in doping level due to increase in dopant molecules. Similarly, for work function 5.2 eV and 5.4 eV as doping concentration increases due to increase in dopant level, threshold voltages also increases. For the study drain voltage is considered as 1 V.

Table 1 ON Current for Different WorkFunctions at Different Doping Level

| DOPING | ON CURRENT | | |
|--------------------------|------------------------|------------------------|------------------------|
| | WF=5.0 | WF=5.2 | WF=5.2 |
| | (ev) | (ev) | (ev) |
| 10^{10}cm^{-3} | 4.28×10^{-12} | 4.3×10^{-12} | 4.31×10^{-12} |
| 10^{11}cm^{-3} | 1.85×10^{-10} | 1.87x10 ⁻¹⁰ | 1.88×10^{-10} |
| 10^{12}cm^{-3} | 1.86×10^{-10} | 1.88×10^{-10} | 1.88×10^{-10} |
| 10^{13}cm^{-3} | 1.85x10 ⁻⁹ | 1.85x10 ⁻⁹ | 1.88x10 ⁻⁹ |
| 10^{14}cm^{-3} | 1.84x10 ⁻⁸ | 1.89x10 ⁻⁸ | 1.9x10 ⁻⁸ |
| 10^{15}cm^{-3} | 1.88x10 ⁻⁷ | 1.89x10 ⁻⁷ | 1.9x10 ⁻⁷ |
| 10^{16}cm^{-3} | 1.82x10 ⁻⁶ | 1.88x10 ⁻⁶ | 1.88x10 ⁻⁶ |
| 10^{17}cm^{-3} | 1.83x10 ⁻⁵ | 1.84x10 ⁻⁵ | 1.85x10 ⁻⁵ |
| 10^{18}cm^{-3} | 0.000175 | 0.000178 | 0.000179 |
| 10^{19}cm^{-3} | 0.00168 | 0.00169 | 0.00171 |

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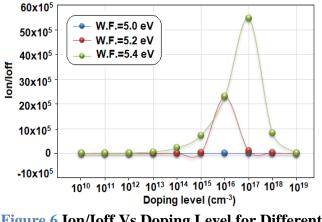


Figure 6 Ion/Ioff Vs Doping Level for Different Work Functions (W.F)

Table1 specifies ON current for different work function values with variation in doping concentration. It can be observed that increasing the doping level the ON current can be increased considering different work functions such as 5.0 eV, 5.2 eV and 5.4 eV respectively. At a doping level of 10^{10} cm⁻³ for work functions 5.0 eV, 5.2 eV and 5.4 eV ON current obtained are 4.28x10⁻¹² A, 4.3x10⁻¹² A and 4.31x10⁻¹² A respectively. On the other hand with increase in doping concentration we obtained ON current of 0.00168 A, 0.00169 A and 0.00171 A respectively. Figure 6 specifies Ion/Ioff ratio for different work function values with various doping concentration level. It has been observed that ON current OFF current ratio increases initially for work function 5.2 eV and 5.4 eV and after a certain doping level it starts decreasing as the off current increases. For work function 5.0 eV Ion/Ioff is very small. Figure 7 specifies Subthreshold Swing for different For the work functions doping level. all Subthreshold Swing increases as the doping level increases. But with work function 5.4 eV Subthreshold Swing has a lesser value compared to the work functions 5.0 eV and 5.2 eV. At a doping level of 10^{19} cm⁻³ for work function 5.4 eV Subthreshold Swing obtained is 75 mV/decade. Subthreshold Swing is calculated by using the formula-

SubthresholdSwing =
$$\frac{\partial V_g}{\partial (\log I_d)}$$

Where dV_g is the change in gate voltage and I_d is drain current.

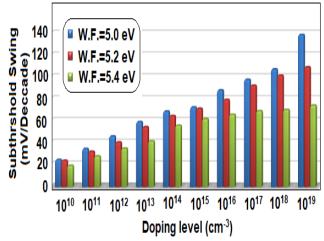


Figure 7 Subthreshold Swing Vs Doping Level for Different Work Functions (W.F.)

The study examines a comprehensive analysis of the effect of work functions on DGJLFET functionality across a wide range of doping profiles, providing a thorough understanding of their interplay. Through the illustration of significant performance achievements, such as the attainment of a threshold voltage of 0.71 V, I_{ON}/I_{OFF} ratio of 3.75, and Subthreshold Swing of 75 mV/decade at specific work function (5.4 eV) and doping levels of 10^{19} cm⁻³, the study highlights avenues for optimizing DGJLFET designs for enhanced functionality and efficiency. **Conclusion**

The present work systematically investigated the impact of work function variations on the electrical performance of conventional Double Gate Field Effect Junctionless Transistors (DGJLFETs) across a range of doping profiles. Through comprehensive analysis of transfer characteristics, On Current, Ion/Ioff ratio, and Subthreshold Swing using TCAD simulation for work functions of 5.0 eV, 5.2 eV, and 5.4 eV were explored in conjunction with doping levels ranging from 10^{10} cm^{-3} to 10^{19} cm^{-3} . The findings reveal that higher doping levels, particularly at 10^{19} cm^{-3} , leads to favorable On Current

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characteristics across varied work function spectra. Notably, a Subthreshold Swing of 75 mV/ decade was accomplished at a work function of 5.4 eV, emphasizing the importance of high work functions in minimizing Subthreshold Swing. In conclusion, the results suggest that DGJLFETs exhibit superior electrical properties, particularly in terms of On Current, when operated with higher work functions. This emphasizes the significance of work function engineering in enhancing the performance of DGJLFET devices.

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