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Implementation of a Static Contention Free Characteristics Differential Flip Flop Using GDI in Clock Gating Technique

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Abstract

This paper introduces the design of a differential flip-flop featuring static contention- free characteristics, achieved through the implementation of a GDI-AND arrangement within a clock gating technique. The proposed approach aims to enhance the reliability and performance of flip-flops in digital circuits, particularly in applications demanding low-voltage and low-power operation. By incorporating a GDI-AND structure in the clock gating technique, contention issues are minimized, ensuring stable and efficient operation. The abstract outlines the design methodology, emphasizing the integration of static contention-free attributes and the innovative use of clock gating with a GDI- AND. This research contributes valuable insights into advancing the design of differential flip-flops, offering improved reliability and efficiency in modern digital systems.

Keywords: *GDI technology, Clock Gating, SCDFF, AND gate, Flip-Flop.*

1. Introduction

The demand for small, portable electronics like laptops, cell phones, palmtops, and other electronic gadgets is primarily driven by four factors in the modern world: area, speed, delay, and power consumption. Previously, the main factors to evaluate were affordability, efficiency, and reliability. But in recent times, integrated circuit designers have given equal weight to issues of power, area, and energy. In the past, speed factors took a backseat to dependability, cost, and performance, with power conservation receiving less attention. In recent years, space and power consumption have become major concerns due to the rising frequencies and chip sizes [1]. Integrated circuit design is done using a process called complementary metal oxide semiconductor CMOS design. The employment complementary semiconductors, such as NMOS and PMOS, is indicated by the prefix complementary to MOS, which refers to MOSFET. Together, these two MOS technologies create a vast assortment integrated circuits and gates [2]. Information-storing devices are necessary for a digital computer. A flip-flop is a circuit that can be used to store state information since it has two stable states. One binary storage device is a flip flop. It is capable of storing binary bits 0 or 1. There are two stable states for it: LOW and HIGH, or 1 and 0. Typically, a clock signal is one of the control signals used to operate a flip-flop. In addition to the conventional output,the complement is typically included in the outputs [3].In digital circuits, flip-flops are essential timing components that significantly affect circuit speed and power consumption[4]. A key factor in determining the overall synchronous circuit performance is the Flip-Flop's performance. FFs has concentrated on creating dependable and low-power circuits, particularly in the NTV area [5][6][7] The following elements are necessary for designing circuits at the NTV region: completely static operation, contention- free transitions, no redundant internal clock transitions to save power consumption, and the least amount of overhead. A static, contention-free differential FF is

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proposed as a solution to this problem. It does this by eliminating dynamic nodes using a ground/supply bridge, removing contention from the differential type FF, maintaining no redundant clock transitions, and maintaining a silicon area comparable to a conventional transmission-gate FF, which has higher power consumption and delay.Of course, a major factor that significantly influences the design complexity of larger circuits is the number of transistors. Topology selection, power dissipation, and speed are crucial factors in this submicron CMOS technology field for high- speed and low-power applications [8]. The application of the Gated Diffusion Input (GDI) technology can resolve these problems. GDI is a method of describing low power digital circuit designs. This method enables the reduction of digital circuit area, latency, and power consumption. While keeping logic design's modest level of complexity.

2. Literature Survey

In 2006. A. Wangnet.al had proposed a system Sub-Threshold Design for Ultra Low-Power Systems. The construction of fundamental components that are present in almost all analog parts of integrated circuits, such as voltage references and operational amplifiers. Ultra-low voltage, extremely low power voltage reference circuits manufactured in the CMOS process were studied in detail, and small signal equivalent circuit parameters were recovered. The novel circuit arrangements enable a notable decrease in the minimum supply voltage and power consumption because theyoperate with all transistors in the sub threshold zone. low-power, low-voltage reference circuit design: in one of the three configurations, the circuit's minimum supply voltage for proper functioning lowers, and its power dissipation is an order of magnitude lower than the best values found in the literature. In 2010, R. G. Dreslinski, et al. Had proposed a system For near-threshold computing, the supply voltage of energy-efficient integrated circuits is about equal to the transistors' threshold voltage, regaining Moore's law. This area has more favorable performance and variability characteristics while retaininga large portion of the energy savings of sub threshold operation. This means that it can be used with a wide variety of power-constrained computer applications, ranging from high-end servers to sensors. This study examines the challenges facing the widespread implementation of NTC and outlines ongoing efforts to surmount them. In 2016, Coping with parametric variation at near-threshold voltages. Since a circuit's supply voltage has a significant impact on its power consumption, aggressive supply voltage scaling to the near-threshold voltage region—also referred to as Near- Threshold Computing (NTC)—is a useful technique for significantly boosting a circuit's energy efficiency. To fully realize the potential of NTC, new design methodologies are necessary because to the unique performance and reliability problems it presents. Cross-layer approaches produce much greater optimizations than strategies that are just focused at one abstraction level, especially in circuit-level design, where the benefits can be limited. In all the above methods having more power consumption and dealay. we describe a novel method for decreasing the power and delay of the circuit

3. Gate Diffusion Input(GDI)

A basic cell is the foundation of the GDI approach. Although there are several significant distinctions, the basic cell bears similarities to the conventional CMOS inverter. The three inputs of the GDI cell are G (the common gate input of nMOSand pMOS), P (the input to the pMOS source/drain), and N (the input to the nMOS source/drain). As seen in Figure 1, bulks of nMOS and pMOS are connected to N or P, respectively, meaning that, in contrast to a CMOS inverter, it can be arbitrarily biased. It should be noted that while some functionalities cannot be implemented successfully in a typical p-well CMOS process, they can be done so in silicon on insulator or twin-well CMOS technologies.

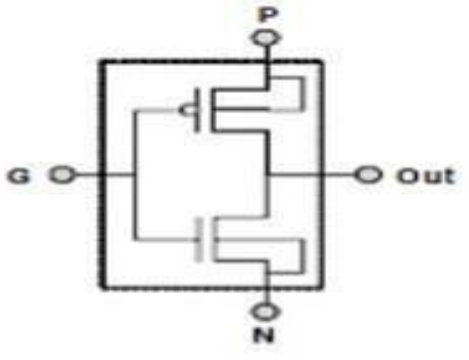

Figure 1 Gate Diffusion Input

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4. Proposed Method

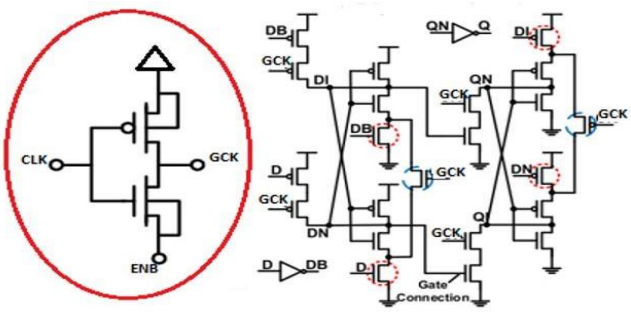

Figure 2 Proposed Diagram

As shown in Figure 2, In Proposed method we are using GDI AND gate for creating the clock pluses for SCDFF. For generating the clock pluses it requires a single GDI cell where port P, the PMOS source, is linked to GND, port G receives input from port A, and port N receives input. As seen in the picture, the clock gating mechanism generates the GCLK. Clock gating reduces power or delay depending on the circuit by requiring an additional logic to provide a clock enabling signal, which is only activated when the circuit design dictates a logic 0 or 1 value. One of the most straightforward methods is gate-based clock gating, which has an easy-to-implement design.

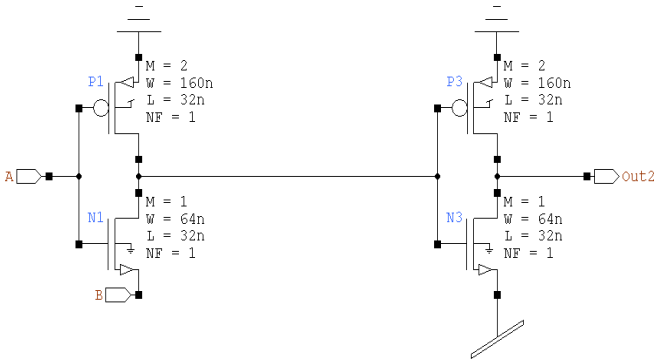

Figure 3 Gated Clock Signal Generated

An SFL can be used as the master latch and a static headed latch as the slave latch to create a SCDFF. The SFLs in the SCDFF, in contrast to the ACFF, are connected by gate connections rather than diffusion connections, enabling completely static and contention-free operation. When the present data (Qprev) and the next data (D) diverge the SCDFF operates in detail. The header cuts off one of the pull-up routes of the back-to-back inverter when GCK = 0, contingent on the DI/DN value. The supply-bridging transistor is still pulling up the current "1" state at QI/QN. Pull up through the bridge is now disabled for the storage node holding "1" (QN or QI) as CK increases, but pull down through the input NMOS stack is activated, leading to a contention-free state toggling. Because the master latch and slave latch share the same form, they function similarly. The SCDFF can operate down to NTV because, as its comprehensive operation demonstrates, it is static and free from contention.

- As shown in figure 3, When GCK=0, Qprev = 0, D=1 then Header blocks pull -up path for the following QN pull- down, GCK rise and supplies power until GCK rise and fully static and retention free.

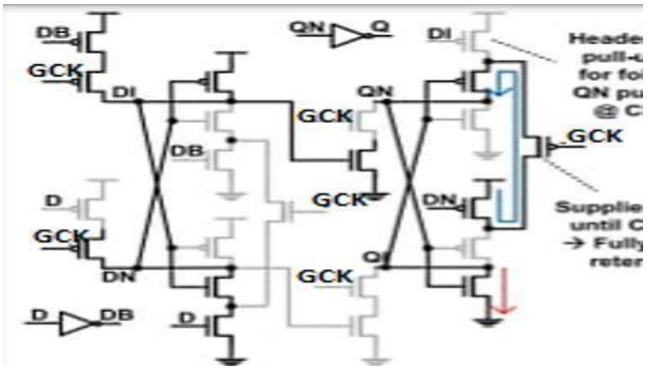

Figure 3 Result 1 When GCK=0, Qprev = 0, D=1

- As shown in Figure 4, When GCK=1, Qprev = 0, D=1 then Clock is disabled, Pull up blocked and contention free and pull down without contention.

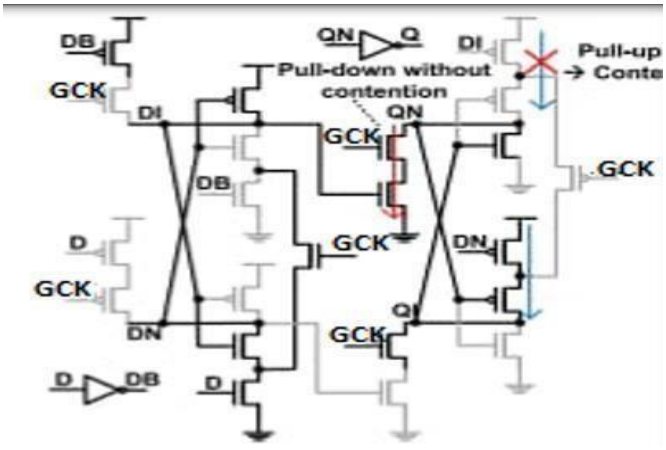

Figure 4 Result 2 When GCK=1, Qprev = 0, D=1

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- As shown in Figure 5, When GCK=0, Qprev = 1, D=0 then Supplies power until GCK rise, Fully static and retention. Header blocks pull-path for following QI pull-down and GCK rise

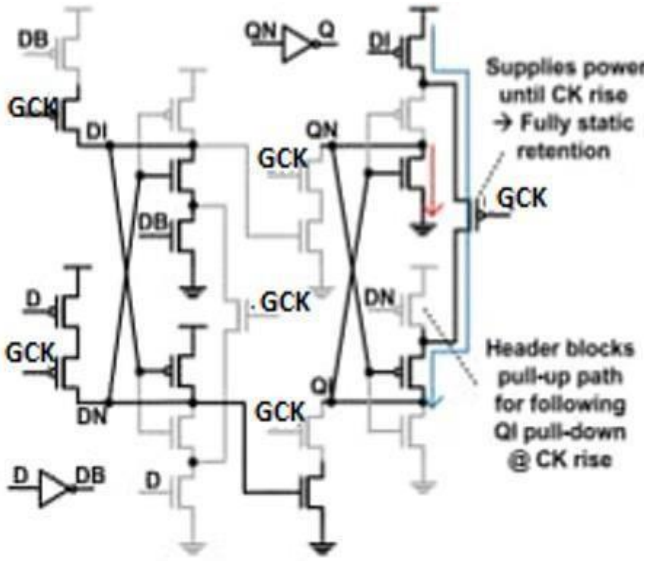

Figure 5 Result 3 When GCK=0, Qprev = 1, D=0

- As shown in Figure 6, When GCK=1, Qprev = 1, D=0 then then Clock is disabled, Pull up blocked and contention free and pull down without contention

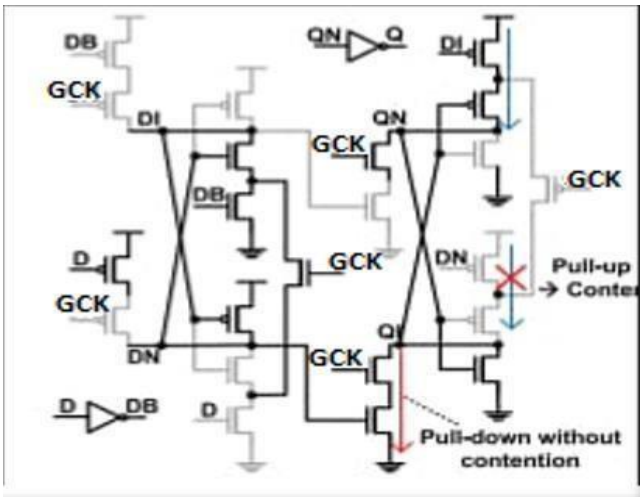

Figure 6 Result 3 When GCK=1, Qprev = 1, D=0

Figure 7 shows Schematic Design of Proposed Design Generated from Tanner EDA and Figure 8 shows Simulation Results of SCDFF Generated from Tanner EDA and Table 1 shows Comparison Results.

5. Simulation Results

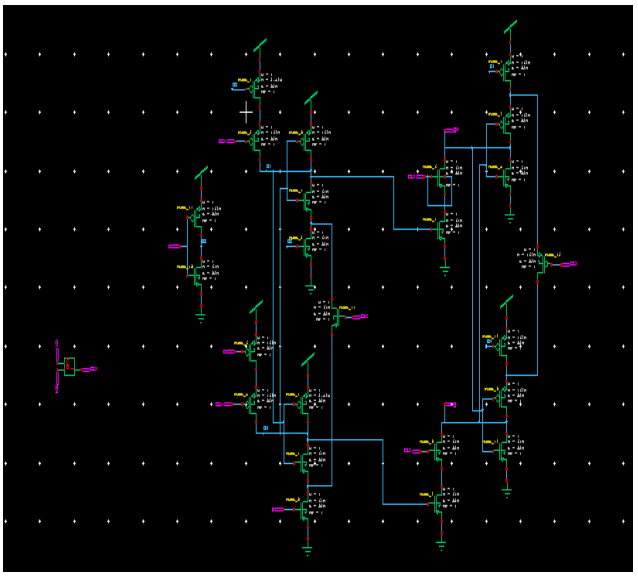

Figure 7 Schematic Design of ProposedDesign Generated from Tanner EDA

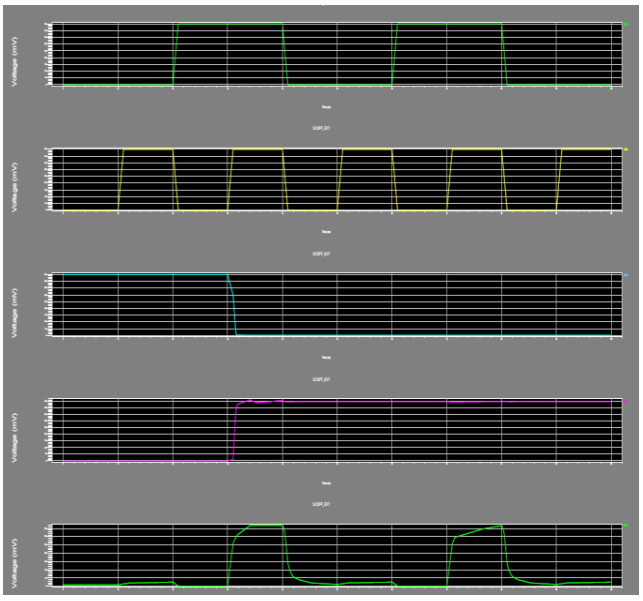

Figure 8 Simulation Results of SCDFF Generated from Tanner EDA

Table 1 Comparison Results

Parameters	Existing	Proposed
Power	5.5 µ	4.63 µ
Delay	10ns	0.2s
Area	24	28

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Conclusion

The outlined design methodology underscores the significance of integrating static contention-free attributes and highlights the novel use of clock gating with a GDI- AND. The findings and insights gained from this research contribute to the ongoing efforts in advancing the design of differential flip-flops, offering practical solutions for improved reliability and efficiency in contemporary digital systems. As digital circuits continue to evolve towards increased energy efficiency and performance, the contributions of this study pave the way for further innovations in flip-flop design methodologies.

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