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Efficient 4-Bit Encoder Design with Memristor Technology and SAPON Integration

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Abstract

This study displays three different encoder setups: CMOS, Memristor, and Pseudo NMOS. Digital logic gate designs that use memristors provide an alternative to the present IC architecture. This computing architecture will be among the upcoming ones. The poly silicon gate of an NMOS transistor can be used to build memristors, making MRL gates simple to fabricate. The encoder's design makes use of four bits. When comparing the recommended 4-bit encoder with memristor logic to one with CMOS logic and pseudo-N MOS logic, the former requires less power. This paper also presents a 4-bit encoder design that combines SAPON methodology with memristor technology, aiming for low-power optimization and increased efficiency. Memristors' dynamic resistance and non-volatile memory enhance encoding performance, minimizing energy consumption and ensuring strategic power optimization. Experimental results demonstrate its potential for efficiency and power conservation.

Keywords: *Encoder, SAPON, combi-national circuits, memristor, and CMOS logic.*

1. Introduction

Soft Moore's rule states that the number of transistors per unit area of semiconductors has been increasing dramatically over the past few decades, about doubling every two years. However, transistor limitations in terms of physical materials, energy consumption, and cost are making the semiconductor field more difficult. Finding a smaller component to replace the typical transistor is one of the numerous solutions put out to maintain Moore's law. The efforts made to create new methods for the CMOS process are very beneficial since there is still a need to achieve a smaller area and better efficiency [1]. The primary problem arises when leakage currents have a greater effect and cause CMOS cells to diminish in size. The dissipation static power is enhanced. The primary problem arises as CMOS cell size decreases due to the significant impact of leakage currents. These leakage currents enhance the static power dissipation. Furthermore, it becomes challenging to build such cells due to the large error rates. By using a passive device called a "Memristor," all of these problems may be resolved and significantly reduced. The concept of a memristor was initially presented by Professor Chua in 1971, and the first memristor at the nano scale was realized by HP Lab in 2008. A range of devices, including FPGAs and amplifiers, have been suggested as potential uses for memristors [2]. Memristors may be used to evaluate a wide variety of memory devices that are utilized in crossbars. Additionally, it makes production easier and addresses regional problems [3].Memristors have several applications in memory, neuromorphic systems, and analog circuits. One interesting application of memristors is in logic, where they are used to construct logic gates. In a digital context, a high memristive is referred to as logic 0, and a low memristive as logic 1 [3]. Among the Memristor logic circuits, Memristor-aided Logic (MAGIC) and Material Implication (IMPLY) Memristor logic are unsuitable because of their complexity and inconsistent numerous fan-outs.

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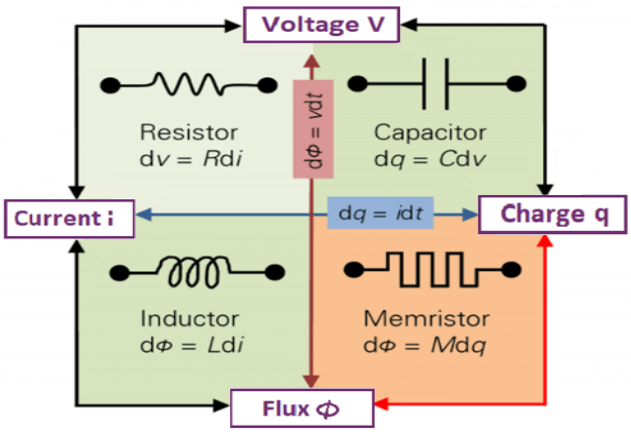

Figure 1 Circuit Model

An encoder is a circuit that is frequently used in digital circuits to encode signals and improve selection ease in digital logic circuits. When creating a logic circuit with a memristor, several logic's can be used. The encoder idea in this study is implemented using Memristor ratioed logic. To compare the new memristor-based encoder with the current CMOS and pseudo-N MOS circuit logic, this research focuses on its design and analysis in terms of power.

2. Working of Memristor

Memristor is just charge-dependent resistance, and an ohm is the memristors unit of measurement. The concept of a memristor was initially introduced from the standpoint of circuit integrity as a hypothetical non-linear passive two-terminal electrical component [1]. Figure 1 and 2 shows Circuit model and Memristor Model.

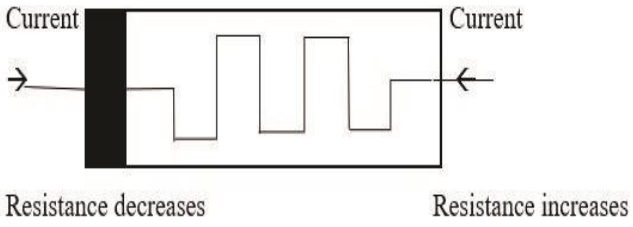

Figure 2 Memristor Model

The relationship between charge and flux is represented by the M = dφ/dq, where M is memristance (ohm), q is charge (coulomb), and φ is magnetic flux (volt-second).The memristor is built in such a manner that pure (undoped) titanium dioxide (TiO2) serves as a dielectric between two platinum metal layers.A semiconductor is formed by doping titanium dioxide (TiO2−x) on top of the dielectric layer. The current through the memristor causes the device's resistance to change [4]. Ron represents low resistance when the width of the doped zone exceeds the width of the undoped region in TiO2. R off is defined as high resistance when the width of the undoped zone exceeds that of the doped region. The dark thick line indicates the polarity of a memristor [5]. When current flows towards the black line, the resistance falls; the lowest resistance provided by the Memristor is known as ON resistance (Ron). As the water travels away from the black line, resistance rises. R off is defined as high resistance when the width of the undoped zone exceeds that of the doped region. The dark thick line indicates the polarity of a memristor [5]. When current flows towards the black line, the resistance falls; the lowest resistance provided by the Memristor is known as ON. Figure 3 shows Memristor Diagrammatic.

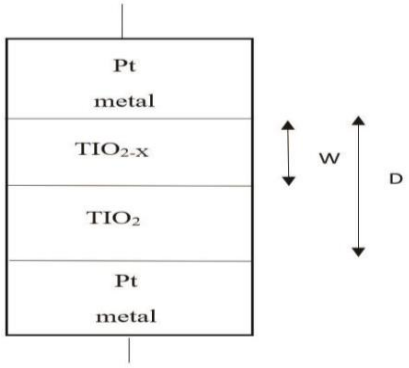

Figure 3 Memristor Diagrammatic

R off, or OFF resistance, is the highest resistance that the memristor can offer. Typically $\frac{R_{off}}{R_{on}} \geq 1000$. In general. Given the Memristor equation, the variable resistance is as follows:

$$R(w) = R_{on}\left(\frac{w}{D}\right) + R_{off}\left(1 - \frac{w}{D}\right)$$

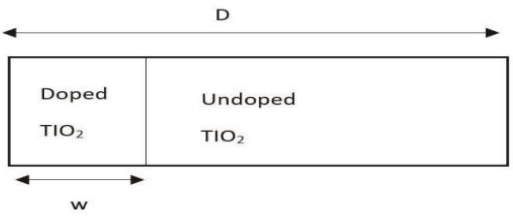

Figure 4 Simple Representation of a Memristor

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In Figure 4, w is the width of the doped TiO2, and D is the overall width of the TiO2. Depending on the supply current, the memristor's undoped width (w) might overshoot or undershoot. Between the Memristor's physical boundaries, the undoped width is controlled by the window function, F(x) [6].

$$x = w/D$$

Here, x represents the ratio of the depletion region's width to the overall TiO2's width.

$$\frac{dx}{dt} = F(x) \times K \times I(t)$$

I(t) is the current at time t, F(x) is the window function, and K is a constant.

$$F(x) = 1 - \left(\frac{2w}{D-1}\right)^{2p}$$

Where p is a positive integer

2.1. Memristor Ratioed Logic

Memristor ratioed logic is the design of logic gates utilizing CMOS technology and memristor (MRL). The advantage over traditional CMOS design is provided by this hybrid design [7]. Memristor can be easily fabricated on top of the CMOS poly silicon layer, which reduces the design's overall area [7]. Additionally, fewer transistors are used [8]. When two memristors, M1 and M2, are connected in parallel in Figure 5, the resultant output is supplied to the CMOS inverter, producing NAND gate logic. The potential across the terminals is zero if we set A=0 and B=0. Subsequently, there is only one CMOS inverter [9].

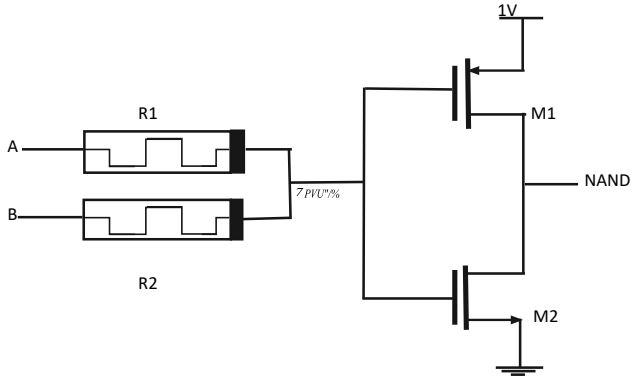

Figure 5 NAND Gate Using Memristor

The NOR gate logic in Fig. 6 can also be obtained by simply inverting the polarity terminals of the memristors in the architecture shown in Fig. 5. When this logic is contrasted with IMPLY and MAGIC logic, the signal attenuation is extremely low [10, 11].

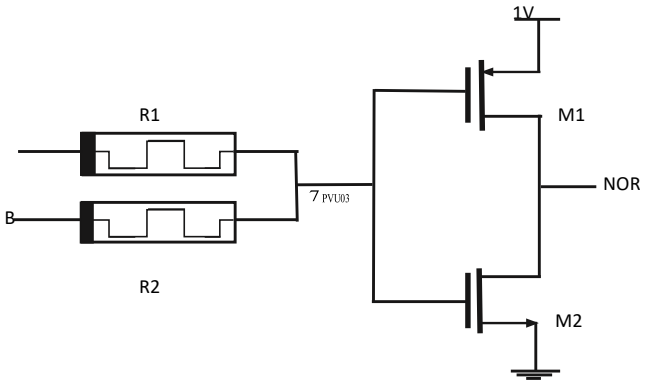

Figure 6 NOR Gate Using Memristor

3. Memristor Models

Memristor research and development is essential to boosting the performance of current-generating circuits. Memristors provide many benefits, including better design density, CMOS compatibility, and non-volatility. Memristors' non-volatility is very inspiring for memory design. Extensive research is being conducted on in-memory computations with the aid of the Crossbar IMPLY logic gate implementation, which is opening the door to a possible revolution in computer architecture known as Beyond-Newman architecture. This could eliminate the V on Newman architecture's existing bottleneck. primarily three models.

3.1. Linear Ion Drift Model

$$R(w) = R_{on}\left(\frac{w}{D}\right) + R_{off}\left(1 - \frac{w}{D}\right)$$

According to this model, the doped region width varies linearly with the input current as

$$\frac{dw}{dt} = \frac{u_v R_{on}}{Di(t)}$$

It is symmetric, simple to use, and makes use of a window function.

$$F(w) = 1 - \left(\frac{2w}{D-1}\right)^{2p}$$

3.2. Simmons Tunnel Barrier

The undoped area width (x) is the state variable in this model.

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$$\frac{dx}{dt} = C_{off} Sinh\left(\frac{i}{i_{off}}\right) \exp\left(\frac{x - a_{off}}{\frac{w_c - |i|}{\left(\frac{b-x}{w_c}\right)}}\right), i > 0$$

$$\frac{dx}{dt} = C_{on} Sinh\left(\frac{i}{i_{on}}\right) \exp\left(\frac{x - a_{on}}{\frac{w_c - |i|}{\left(\frac{b-x}{w_c}\right)}}\right), i < 0$$

This model has higher complexity and asymmetric switching timings, and it is accurate.

3.3. Threshold Adaptive Model (TEAM)

The state variable in the TEAM model is the undoped area width. It uses current thresholds and allows parameters to be changed for other models. It takes advantage of window functions and offers acceptable [12] accuracy with less complexity.

$$\frac{dx}{dt} = k_{off}\left(\frac{i(t)}{i_{off} - 1}\right)^{a_{off}} f_{off}(x),\ 0 < i_{off} < i$$

$$\frac{dx}{dt} = 0 \quad ,\ i_{on} < i < i_{off}$$

$$\frac{dx}{dt} = k_{on}\left(\frac{i(t)}{i_{on} - 1}\right)^{a_{on}} f_{on}(x),\ i < i_{on} < 0$$

The current is modeled as

$$V(t) = R_{on} i(t) \exp\left(\frac{y}{(x_{off} - x_{on})(x - x_{on})}\right)$$

$$\frac{R_{on}}{R_{off}} = e^{y}$$

3.4. Window Function

There is a possibility that the Memristor's breadth will exceed its actual size. Therefore, we constrain the width to be inside the Memristor's physical dimensions using window functions for simulation. Numerous window function models are available, including Biolek, Joglekar, and others [10], [12]. This work uses the Joglekar window function of memristors and the Ion Drift Model to model an encoder.

4. Encoder Design and Operation

Binary bits that correspond to specific meanings are used in digital logic circuits to encode data. The circuit that performs this encoding function is called an encoder. When one of the input bits is at an effective level, the encoder's job is to encode; its output varies based on the bits it receives. The relationship between the circuit's "N" outputs and "M" inputs is given by M = 2N. The encoder diagram and its truth table are displayed in Figure 7 and Table I, respectively. The outputs and inputs are connected by the encoder truth table. From the Encoder truth table, the outputs and inputs are related by

O0 = X1 + X3 + X5 + X7 + X9 +X11+X13+X15
O1 = X2 + X3 + X6 + X7 +X10+X11+X14+X15
O2 = X4 + X5 + X6 + X7+X12+X13+X14+X15
O3 = X8 +X9+X10+X11+X12+X13+X14+X15

From these relations, a logic circuit can be implemented using CMOS and MRL. In the Encoder circuits, X1- X7 are input bits and O3, O2, O1, and O0 are output bits. In an Encoder circuit using MRL, MOS transistors act as a pull-down network and a Memristor acts as a pull-up network. MOSFETs and Memristor constitute a 4-input NOR gate. X1, X3, X5, and X7…. respectively are the input signals that pass through the NOR gate and the signal at the drain of MOS is an inverted signal of (X1 + X3 + X5 + X7+ X9 +X11+X13+X15). NMOS and Memristor constitute an inverter. The output of the 4-input NOR gate is given as the input of the inverter. The signal at the output node is O0 = X1 + X3 + X5 + X7 + X9 +X11+X13+X15.

Table I Encoder Truth Table

						Inputs										Outputs			
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

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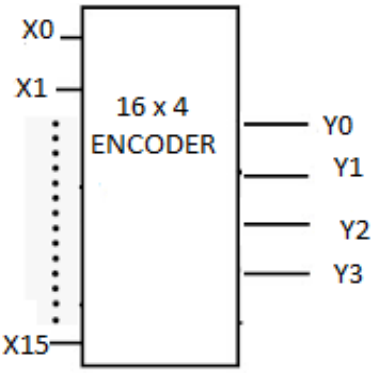

Figure 7 4-Bit Encoder

5. Results and Discussion

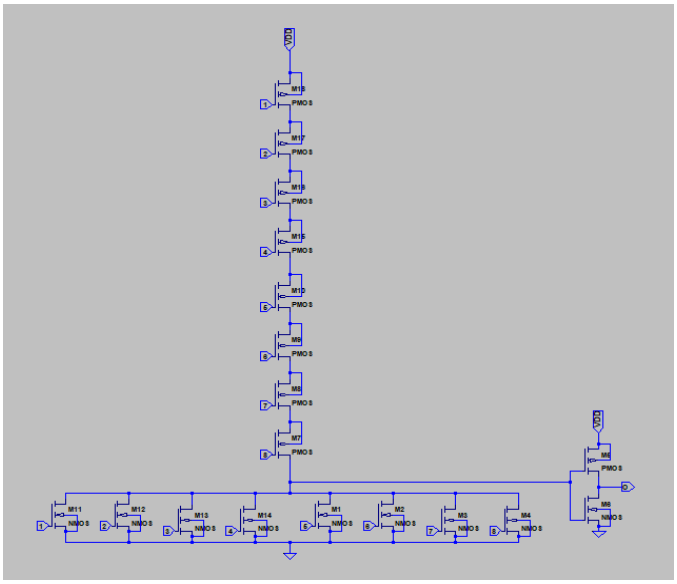

Figure 8 Schematic of 8-Bit OR Using Memristor-Based Logic

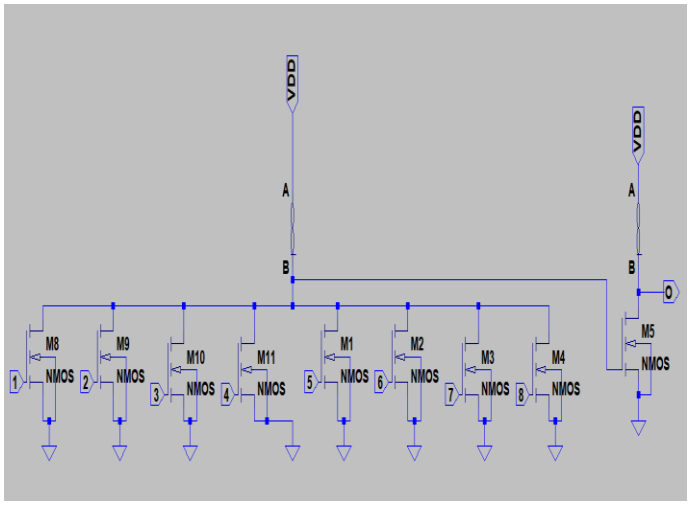

Figure 9 Schematic of 8-bit OR using CMOS Logic

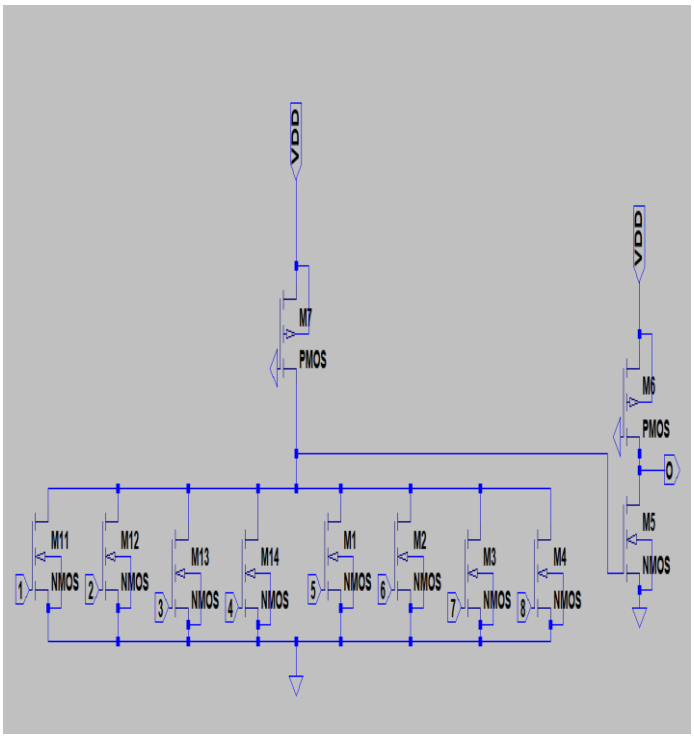

Figure 10 Schematic of 8-Bit OR Using Pseudo NMOS

The results are shown in Figure 8, 9, 10. Memristor-based designs are known to occupy less area than CMOS designs [11], [14], and [15]. Therefore, it can be inferred that their efficiency in terms of area consumed is high. When compared to traditional CMOS logic, it is evident that this design requires the fewest transistors overall. The encoder circuit contains 72 transistors (36 PMOS and 36 NMOS) thanks to CMOS technology. The encoder has 36 transistors total—8 memristors and 36 NMOS—thanks to MRL technology.

5.1. SAPON Approach

As shown in Figure 11, A stack of leakage-controlled transistors positioned below the circuit makes up a stackable arranged low-power ON transistor or SAPON. The gate of the PMOS leakage-regulated transistor is grounded. As seen in the figure, the gate of the NMOS leakage-regulated transistor is connected to Vdd; as a result, both leakage-controlled transistors will function in the active region. Although a transistor's resistance in the active region is less than that in the cut-off region, this little resistance will still contribute to a decrease in power consumption.

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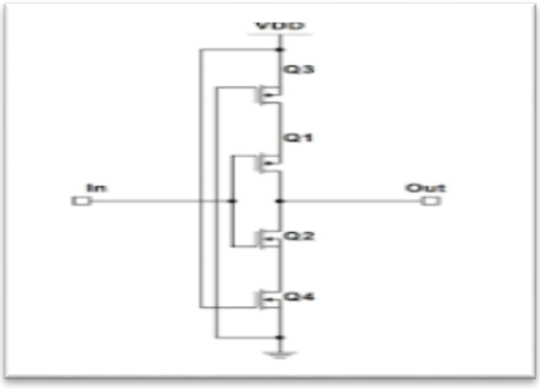

Figure 11 Block Diagram of SAPON

5.2. Proposed OR Design

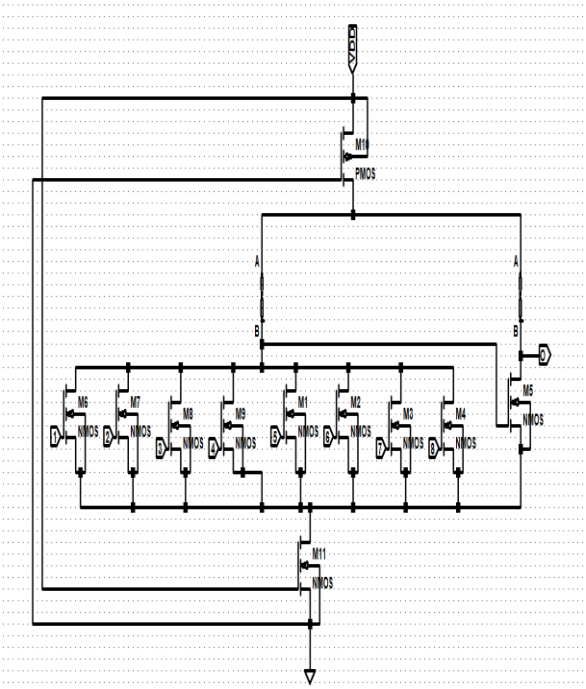

Figure 12 Proposed OR Logic Gate Using SAPON and Memristor

It is possible to conclude from looking at the proposed structure and the SAPON Block diagram that the M10 and M11 make up the SAPON network, and the remaining structure will stand in for the MRL OR circuit. As M10 is PMOS and M11 is NMOS, the gate terminals of both transistors are connected to GND and vdd, respectively, upon circuit analysis. This indicates that both transistors are always in the ON state. Figure 12 shows Proposed OR Logic Gate Using SAPON and Memristor.

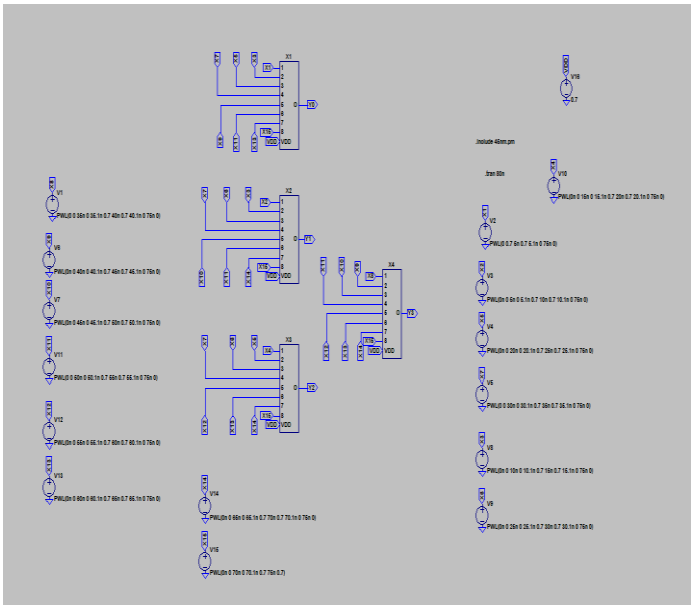

Figure 13 Block Diagram of the Encoder Using LT-Spice

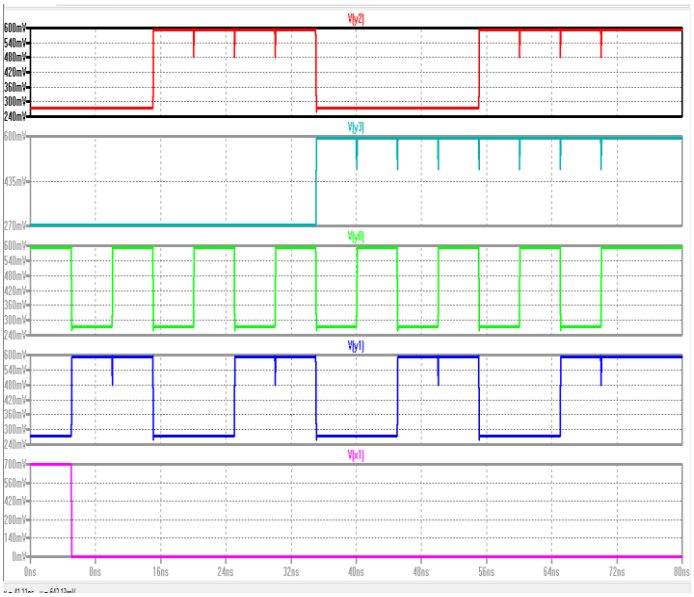

Figure 14 Output Waveforms in LT-Spice

Table 2 Comparison of Performance Parameters among CMOS, Pseudo NMOS, and MRL-Based Encoders

	Average Power	Delay
CMOS based encoder	205 µW	184.33ps
MRL based encoder	170 µW	61.4439ps
Pseudo NMOS encoder	2.7 mW	61.8238ps
Proposed Encoder	89.8 µW	20.433ps

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Conclusion

The addition of SAPON emphasizes the dedication to strategic power optimization even more by making sure that energy usage is kept to a minimum while encoding data. In addition to increasing efficiency, this novel use of memristors and SAPON shows great promise for applications that need to strike a careful balance between advanced functionality and power saving. The proposed 4-bit encoder design is effective, as demonstrated by the experimental results, and it can fulfill the requirements of a variety of applications that value low power consumption and efficiency. In addition to advancing the field of encoder design, this research establishes a standard for integrating cutting-edge technologies and power optimization techniques in digital systems. The results open new possibilities for understanding low-power encoder design principles and practical applications. Figure 13 shows Block Diagram of the Encoder Using LT-Spice and Figure 14 shows Output Waveforms in LT-Spice. Table 2 shows the Comparison of Performance Parameters among CMOS, Pseudo NMOS, and MRL-Based Encoders.

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