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# Low-Power 12T SRAM with Improved Read Stability, Multi-Node Upset Recoverability and Soft-Error Mitigation for Aerospace Applications

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## Abstract
*Transistor sizes are getting smaller as technology advances, which lowers the critical charge in SRAM cells used in aircraft. This increases their vulnerability to soft mistakes, in which radiation can cause SEUs by flipping stored data. We suggest the Soft-Error-Aware Read-Stability-Enhanced Low Power 12T (SARP12T) SRAM cell as a solution to this problem. When it comes to soft-error cells, SARP12T guarantees data recovery even in the face of radiation damage, including single-event multi-node upsets, in contrast to QUCCE12T and RSP14T. It has exceptional read stability and uses the least amount of hold power to recover from disruptions during read operations. Though it uses slightly more energy and has a little longer read latency, SARP12T excels in write capabilities and delay. Its advantages promise improved performance and dependability in crucial systems, extending to CPU and aircraft applications.*

***Keywords:*** *Read stability, low power consumption, soft error awareness, SRAM cell, aerospace applications.*

## 1. Introduction

The performance and dependability of SRAM cells are seriously jeopardized by soft mistakes, sometimes referred to as single-event upsets (SEUs), particularly in radiation-exposed aerospace applications. The traditional 6T SRAM cell is especially susceptible to radiation-induced soft errors because it uses two weakly cross-coupled inverters for state retention and access transistors for read and write operations. The purpose of this study is to improve memory storage reliability in aerospace contexts by proposing the SARP12T cell as a solution to these problems. The cross-coupled inverters store the data, and the write operation in the present 6T SRAM cell design entails driving data and its complement into the bit lines and raising the word line to start the write process. Bit lines are first pre-charged high during read operations and are then permitted to float. The stored data value is indicated by the bit line bar being pulled down by the elevated word line. Nevertheless, because of its intricate access transistor architecture, the 6T SRAM cell has many disadvantages, most notably its vulnerability to soft mistakes and considerable read and write operation delays. To address these problems, improvements are introduced in the SARP12T SRAM cell. First off, by adding more transistors and capacitors, it strengthens resistance to disturbances caused by radiation and lowers the frequency of soft errors, both of which contribute to improved read stability. Second, improved reliability in aerospace conditions is ensured by the SARP12T cell's ability to recover from single-event multi-node upsets (SEMNU), in contrast to the conventional SRAM cell. Lastly, despite the added components and improved functionality, the SARP12T SRAM cell maintains low power consumption, making it suitable for energy-constrained aerospace applications. the SARP12T SRAM cell presents a promising solution to address the challenges posed by soft errors in aerospace contexts. By bolstering read stability, enabling SEMNU recovery, and minimizing power consumption, the SARP12T cell enhances memory system reliability and performance in radiation-intensive environments, safeguarding critical data integrity in space missions and other aerospace endeavors.

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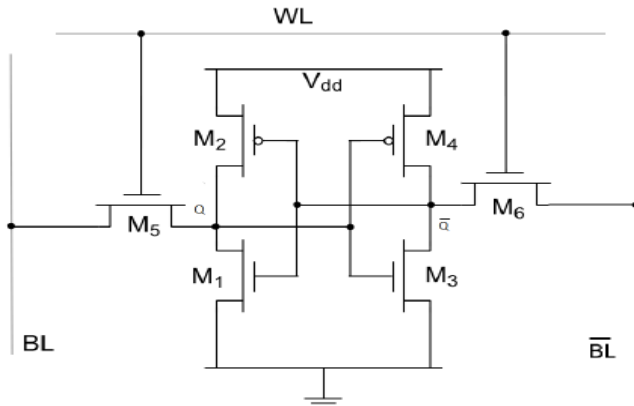


**Figure 1 Conventional 6T SRAM**

## 2. Review of Literature

**Pal et al. (2020):** For space applications, Pal et al. suggest a Half-Select-Free Low Power Dynamic Loop-Cutting Write Assist SRAM Cell. Their primary objective is to minimize power consumption without compromising dependability, a crucial consideration in aeronautical systems.

**Pal et al. (2021):** This paper presents a soft-error aware SRAM design with multi-node upset recovery specifically tailored for aerospace applications. The authors emphasize the importance of mitigating radiation-induced disturbances to enhance memory reliability in harsh environments.

**Peng et al. (2019):** Peng and co-authors introduce a radiation-hardened 14T SRAM bitcell optimized for speed and power in space applications. Their work highlights the significance of addressing both reliability and performance requirements in aerospace memory design.

**Jahinuzzaman et al. (2009):** This study presents a soft-error tolerant 10T SRAM bit-cell with differential read capability. The authors focus on enhancing data integrity and reliability by incorporating error-tolerant features into the SRAM cell design.

**Dang et al. (2017):** Dang, Kim, and Chang introduce the We-Quatro SRAM cell design, emphasizing parametric process variation tolerance. Their work demonstrates the importance of designing SRAM cells resilient to process variations for reliable operation in terrestrial applications.

**Pal et al. (2021):** Pal et al. present a soft-error resilient read decoupled SRAM with multi-node upset recovery specifically designed for space applications. Their work focuses on enhancing memory resilience to radiation-induced disturbances, ensuring reliable operation in harsh environments.

**Qi et al. (2016):** In order to tolerate single-event upsets, this study presents a highly dependable memory cell architecture along with layout-level techniques. The significance of layout optimization in improving memory reliability in radiation-intensive situations is emphasized by the authors.

**Prasad et al. (2020):** Prasad, Mandi, and Ali propose a power-optimized SRAM cell with high radiation hardening for aerospace applications. Their research highlights the significance of power efficiency and reliability in aerospace memory design.

**Pal et al. (2020):** Pal and colleagues present a highly stable low-power radiation-hardened memory-by-design SRAM for space applications. Their work emphasizes the importance of stability and reliability in SRAM cell design for aerospace systems.

**Pal et al. (2019):** Pal and co-authors characterize a Half-Select-Free Write Assist 9T SRAM Cell, focusing on improving write stability and reducing power consumption. Their research contributes to the development of low-power SRAM cells suitable for space applications.

**Pal et al. (2020):** In this study, Pal et al. propose a highly stable reliable SRAM cell design for low-power applications. Their work underscores the importance of stability and reliability in SRAM design for energy-efficient systems.

**D'Alessio et al. (2014):** D'Alessio, Ottavi, and Lombardi present the design of a nanometric CMOS memory cell hardened to single events with multiple-node upsets. Their research highlights the importance of designing SRAM cells resilient to single-event upsets for reliable operation in radiation-intensive environments. The literature analysis indicates that there is a significant focus on improving the power efficiency, stability, and dependability of SRAM cells for aerospace applications. This is especially true when it comes to reducing disturbances caused by radiation. The research provides significant understanding into the development and enhancement of SRAM cells that are customized to meet the specific needs of aerospace and space applications.

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## 3. Methodology

This paper describes a methodology for designing, simulating, and comparing various CMOS technologies (65nm, 45nm, and 18nm) Tanner EDA-based SARP12T cells. The objective of this strategy is to improve read stability and facilitate recovery from radiation-induced SEUs, hence mitigating the vulnerabilities of standard 6T SRAM cells. Evaluation of performance parameters including area along with delay and power consumption is done through comparison with current soft-error SRAM cells. The design optimization of the SARP12T SRAM cell to reduce soft errors and boost overall performance is its primary innovation.

## 4. Design and Simulation

The design and simulation process involve leveraging Tanner EDA to implement the SARP12T SRAM cell architecture across different CMOS technologies. This entails translating the conceptual design of the SARP12T SRAM cell into a physical layout and simulating its performance under various operating conditions and environmental factors.

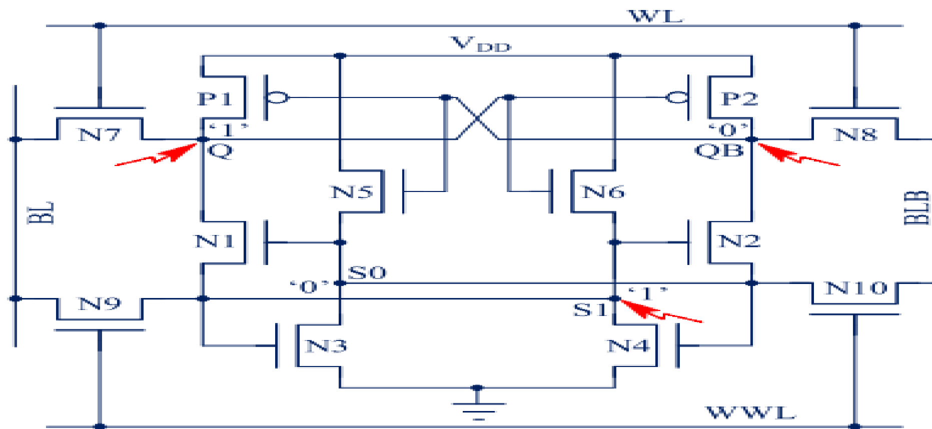


**Figure 2** Schematic of the Proposed SARP12T SRAM Cell

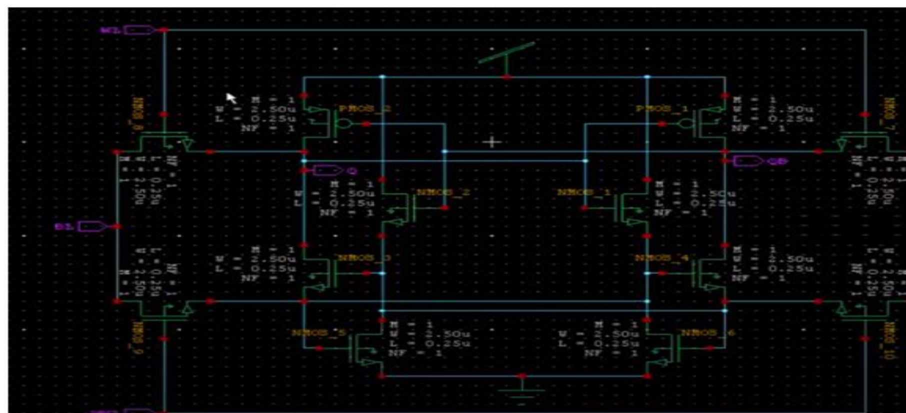

**Figure 3** Simulation Design

**Read Stability Enhancement:** The primary focus of the SARP12T SRAM cell design is to enhance read stability, particularly in the presence of radiation-induced disturbances. This is achieved through architectural optimizations and circuit-level enhancements that improve the robustness of the cell's read operation. By ensuring greater stability during read operations, the SARP12T SRAM cell reduces the susceptibility to soft errors, thereby enhancing the reliability of memory storage in radiation-intensive environments such as aerospace applications. Figure 2 shows Schematic of the Proposed SARP12T SRAM Cell and Figure 3 shows Simulation Design [6-10]

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**Multi-Node Upset Recovery:** Another key feature of the SARP12T SRAM cell is its capability to recover from single-event multi-node upsets (SEMNU). Unlike traditional 6T SRAM cells, which may suffer from data corruption or loss in the event of a single-node upset, the SARP12T SRAM cell is designed to detect and recover from upsets affecting multiple nodes simultaneously. This ensures data integrity and minimizes the impact of radiation-induced disturbances on memory content. [11-14]

## 5. Results

According to simulation data, the SARP12T SRAM cell performs better in terms of read stability, write ability, and hold power consumption than the current soft-error-aware SRAM cells. SARP12T has excellent reliability and efficiency, which makes it a good choice for aerospace applications, despite a little longer read delay and somewhat greater read and write energy consumption. Figure 4 shows the Voltage Graphs and Table 1 represent the Comparison Table.

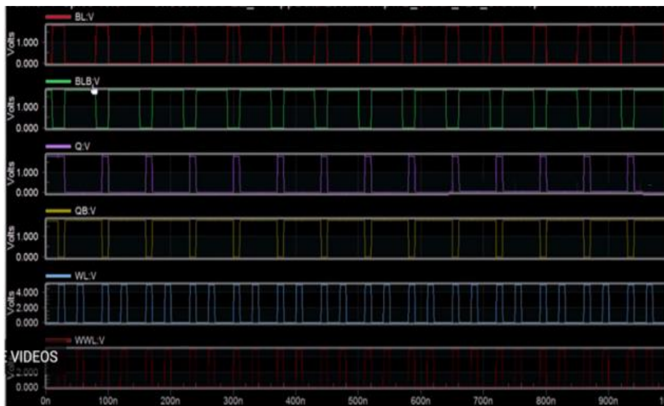


**Figure 4** Voltages graphs

**Table 1** Comparison Table

| | Comparison of Soft Error Read Stability Enhanced Low Power 12T SRAM | | | |
|---|---|---|---|---|
| | 12T SRAM 65 nm | | 12T SRAM 45 nm | |
| | 1 BIT SRAM | 8 BIT SRAM | 1 BIT SRAM | 8 BIT SRAM |
| MOSFETs | 12 | 112 | 12 | 112 |
| Area (um) | 0.780 | 7.280 | 0.540 | 5.040 |
| Average Power (uW) | 11.550 | 631.03 | 0.3381 | 31.8857 |

## Conclusion

In this short, we propose SAR14T, a Soft-Error Aware Read-Decoupled SRAM cell designed for application in aerospace. From SEU of any strength and polarity, the sensitive nodes of the suggested cell can recover. Additionally, after SEMNU is generated at its internal node pair, SAR14T is likewise capable of full recovery. For maximum read stability, it makes use of the read decoupling approach. It additionally displays the shortest TWA and the maximum writing ability. However, the maximum EQM displayed by SAR14T indicates its advantage over the other comparison cells. For applications involving aircraft, SAR14T turns out to be a superior SRAM cell option.

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