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Digital Aided Analog Data Acquisition for Telemetry

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Abstract
This paper tackles the limitations in the current data acquisition system through the integration of a equiripple Finite Impulse Response (FIR) filter. The inclusion of this digital filter eliminates the necessity for physical component alterations, thereby increasing the system's adaptability and versatility in telemetry applications. The FIR filter's ability to adjust passband, stopband, and sampling frequencies allows for seamless reconfiguration without the need for hardware modifications, representing a substantial enhancement compared to the constraints of the previous system. Additionally, the equiripple design guarantees minimal variations in passband and stopband ripples, thereby optimizing overall filter performance. An important aspect of the proposed solution is the implementation of shift-and-add multiplier architecture for the FIR filter, which contributes to a reduction in hardware complexity and resource requirements, ultimately leading to a more efficient system. The adoption of MATLAB's robust filter design tools, coupled with subsequent verification through SIMULINK simulations, has played a pivotal role in successfully realizing the proposed design. To sum up, this project has efficiently addressed the identified issues by introducing a reconfigurable FIR filter solution that not only enhances the flexibility, performance, and user friendliness of the data acquisition system in telemetry applications but also showcases the potential for broader applications in various signal processing domain.

Keywords: *Data Acquisition System; FIR filter; Reconfiguration, Telemetry applications; Shift-and-add multiplier architecture.*

1. Introduction
Data acquisition systems (DAS) gather data (sensors) and convert it to digital form (ADC) for analysis. They are crucial in various fields like telemetry, where sensors capture data, it's conditioned (filtering, amplification), converted to digital (ADC), transmitted (radio, satellite), stored (data logger), and analyzed. The structure of a basic DAS is shown in Figure 1. The key components of the system include, sensors to convert physical parameters (temperature, pressure) to electrical signals, signal conditioning block to prepare raw signals for accurate measurement (amplification, filtering), an anti-aliasing filter to prevent signal distortion during conversion (removes high-frequency noise) and finally the analog-to-digital converter (ADC) that converts analog signal to digital data. Among various ADCs the Sigma-Delta ADCs excels in low-frequency signals. There is a computer in the basic block diagram to analyze, display, and stores data for real-time monitoring and decision-making.

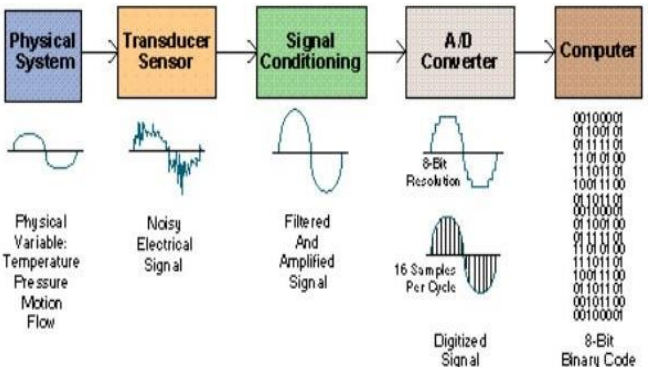

Figure 1 Basic Data Acquisition System (DAS)

1.1. Role of Sigma-Delta ADC
A Sigma-Delta Analog-to-Digital Converter (ADC) is a key component in data acquisition systems for telemetry [1] applications. This type of ADC employs a technique that oversamples the input signal, providing high resolution and accuracy. Sigma-Delta ADCs [2] utilize a feedback loop to continuously

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compare the incoming analog signal with a quantized version, producing a stream of high-frequency, oversampled data. This data is then filtered and decimated to yield a high-resolution digital output. A typical data acquisition system comprises sensors/transducers, signal conditioning, analog-to-digital converter (ADC), and data communication/storage components. In telemetry, Sigma-Delta ADCs [2] excel in capturing low frequency signals with precision, making them suitable for applications where signal integrity is crucial. Their inherent ability to suppress noise and interference enhances the overall reliability of data collected from remote or challenging environments. The Sigma-Delta ADC's design contributes to its efficiency in telemetry, offering a balance between resolution, speed, and power consumption, making it a preferred choice for demanding data acquisition scenarios in aerospace, environmental monitoring, and other telemetry applications.

1.2. Problem Definition

Currently, to make adjustments on various parameters like the sampling rate, passband frequency, and stopband frequency in typical data acquisition systems physical alterations to resistor and capacitor values have to be done. This introduces practical constraints and limitations in adapting the system to varying telemetry signal requirements. The identified limitation in the frequency response of the existing data acquisition system poses a significant challenge in telemetry applications. To overcome this challenge, a proposed solution involves integrating a Finite Impulse Response (FIR) filter [3-4] into the system. The FIR filter aims to address the limitations by providing flexibility in adjusting filter characteristics without the need for physical component changes, thereby enhancing the adaptability and performance of the data acquisition system in telemetry applications. The remaining sections of this paper is structured as follows:

2. Proposed Solution

In the current data acquisition system, adjusting parameters such as sampling rate, passband frequency, and stopband frequency necessitates physical alterations to resistor and capacitor values, introducing practical challenges. The proposed project aims to address this limitation by designing a compensatory Finite Impulse Response (FIR) filter with configurable passband, stopband, and sampling frequencies, eliminating the need for physical component changes. Furthermore, the system employs an equiripple filter to limit variations in passband and stopband ripples, ensuring enhanced filter performance.

2.1. Reconfigurable FIR Filter

Unlike the existing system, which requires manual adjustments of physical resistors and capacitors for passband frequency setting, the proposed design introduces a reconfigurable FIR filter in the digital domain. This filter not only allows for parameter changes such as sampling, passband, and stopband frequencies but also allocates more frequency in the passband than required, ensuring flexibility. Additionally, the proposed FIR filter features a sharp 50 dB roll-off, providing improved signal processing capabilities. In contrast to the current system's limitation of being applicable only to a specific frequency, the proposed equiripple FIR filter allows for a range of decimation factors (from 1024 to 2) through a designed decimator. This innovation enables the selection of diverse sampling, passband, and stopband frequencies, rendering the system versatile and adaptable to varying telemetry signal requirements. The result is a comprehensive solution that enhances the flexibility, performance, and ease of use of the data acquisition system in telemetry applications.

2.2.Use of Less Resources

The use of less resources is a major concern of the system under consideration [5]. The proposed design entails the implementation of a Finite Impulse Response (FIR) filter using a Shift and Add multiplication technique. This approach relies on addition for multiplication, making it a straightforward and cost-effective solution, particularly suitable for data acquisition systems in low-frequency instrumentation applications. The versatility of this method extends to FPGA-based systems, where its multiplier-less architecture offers advantages such as reduced hardware complexity and supporting a broader signal bandwidth. In this implementation, the emphasis lies on avoiding complex hardware computations, specifically eliminating multiplications. If multiplication is

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deemed necessary, it is achieved through shifting the register data. To address the suboptimal passband characteristics of the sinc filter in data acquisition systems, a 60-order filter is implemented. Notably, the realization of this filter only requires adders and shifters, eliminating the need for complex computations or intricate structures.

3. Methodology

The block diagram of the proposed design methodology is shown in Figure 2.

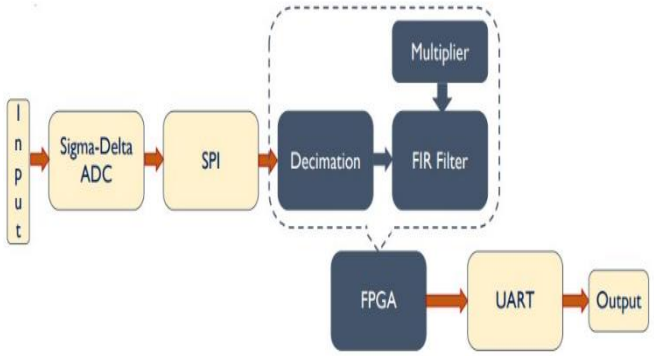

Figure 2 Proposed Design

In proposed design a FIR Filter is added after the ADC. The filter is equiripple with a passband attenuation of 0.2 and stopband attenuation of -50dB. The roll-off of the filter is very sharp. Hence, by allowing an extra margin of frequency into the passband we can obtain the required range of frequencies with lesser noise. Also, the sampling frequency, passband frequency and stopband frequency of FIR Filter can vary in digital domain without physically varying the capacitance and resistance [3]. The method of selecting passband and stopband frequencies is discussed below. This eliminates the need for reworking the circuits according to the various areas in which the system is implemented. In FIR Filter the multiplication is done by using shift and adder. By using the adder block for doing multiplication, the resources needed for computation are reduced greatly, thus making the system more efficient. Initially, a signal of higher frequency is provided as the input. As the roll-off of the FIR filter is sharper than the sinc filter, this enables us to get the required frequency through the passband without signal loss. The data from the Sigma-Delta ADC goes through a decimation unit where it is decimated by a factor of 32 (smallest experimental value between 31 and 1024). This is the data rate. The passband and stopband frequency can be determined using the following equations:

Passband frequency = (Data Rate * 0.205)

Stopband frequency = (Data Rate * 0.5)

Based on these values, the sampling frequency is determined. By entering these values in MATLAB, the required filter's coefficients are generated automatically using the filter designer app.

3.1.Design of Optimized N-Tap Filter

MATLAB streamlines FIR filter design. Users define filter type, cutoff frequencies, and desired order using functions like fir1 or firpm. Iterative refinement with functions like filter or fvtool optimizes filter performance. Complex designs leverage the Parks-McClellan algorithm (firpm). Key specifications include sampling frequency (fs), passband (fpass), stopband (fstop), passband ripple (Ap), and stopband attenuation (Ast). The firpm function designs the filter based on these parameters and aims for an equiripple response. The chosen design approach, achieved with 60 coefficients (60th order), translates to 60 multipliers, 59 adders, and 59 delay units. However, for hardware implementation, filter coefficients need conversion from double-precision floating-point to a fixed-point format with reduced bit-width (e.g., 1-bit exponent, 15-bit mantissa). Finally, the designed filter is exported to Simulink for further analysis.

3.2.Simulation of the Designed Filter

SIMULINK, an integral part of MATLAB, offers a robust simulation environment for analyzing system performance. It provides a visual platform for modeling complex dynamic systems, making it ideal for filter analysis. Simulation involves constructing a block diagram representing the decimation system, including components like the input signal source, digital filter, down sampling operation, and subsequent processing stages. Within SIMULINK, key parameters such as filter coefficients and tap quantization levels can be defined. Real-time visualization enables the observation of filter frequency response, down sampling effects, and overall system behavior, aiding in issue identification and resolution. Parameter adjustments allow for

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exploration of filter configurations and sensitivity analysis, providing valuable insights into system robustness.

3.3.Design of Shift and Adder Multiplier Using Verilog

a. Using Shift and Add Multiplier in FIR Filter*:*

In FIR filters, the shift-and-add operations play a vital role in the streamlined implementation of the convolution process [6]. FIR filters necessitate multiplying input samples by filter coefficients and summing the results, which is a task efficiently handled by the shift-and-add approach. The process involves systematically shifting input samples and coefficients through stages, performing binary multiplications using shift-and-add circuits. The simplicity and speed of this operation make it ideal for hardware implementations, reducing complexity and resource requirements. In FIR filters, the shift-and-add methodology is a cornerstone for achieving convolution with precision and efficiency, making it a fundamental technique in various digital signal processing applications, from audio processing to communication systems. The aforementioned multiplier was implemented using Verilog code in Libero SoC. It takes data in the form of 2 16- bit binary values as well as a clock, control and reset signal for integration to the top module and for user understanding. The output is provided as a 32-bit value along with a flag to show completion of operation. The multiplier uses a state variable to increment each shift of the bit during operation.

b. Testing Shift and Add Multiplier Using Test Bench:

The test bench serves as a controlled environment where the multiplier is subjected to various input scenarios. Test vectors, representing different sets of input values, are applied to the multiplier, and the resulting outputs are compared with pre-computed or ideal results. This verification process helps identify and rectify potential errors or discrepancies in the multiplier's operation. Test data at this stage involved a series of testing using combinations of various bit values and verifying the answers manually when simulation was done. Once the multiplier was integrated into the filter, the test data was again generated by MATLAB as a series of sine wave values from the addition of one wave of frequency within the passband and another noise signal. These were stored into a text file and were used for testing the working of the multiplier.

4. Simulation Platforms Used

4.1.Libero SoC

Libero SoC, a software suite for FPGAs by Microchip Technology, targets SmartFusion2 and IGLOO2 families, offering a complete FPGA development flow. It includes tools for design entry, synthesis, place and route, simulation, and implementation. Filter implementation in Libero SoC can be done through pre-built IP cores like Core FIR and Core IIR, or custom-designed using Verilog or VHDL. The chosen approach for the project was HDL Implementation.

4.2.Smart Fusion

Microchip Technology's Smart Fusion FPGAs combine FPGA fabric with an ARM Cortex-M3 processor, offering a versatile System-on-Chip (SoC) solution. Key features include programmable logic fabric for customizable digital circuits, an embedded ARM CortexM3 processor for control algorithms and data processing, and integrated peripherals such as memory, communication interfaces, and timers, streamlining system design.

4.3.Simulink

Utilizing Simulink for Digital-to-Analog Converters (DACs) provides engineers a versatile platform for modeling and validating signal processing systems. In Simulink, engineers can visually construct block diagrams representing DAC components, including filters and signal sources [7]. Simulink's wide array of signal processing blocks allows seamless integration of DAC functionalities, including custom algorithms and behavioral models. This flexibility is beneficial for tailoring DAC designs to specific applications and assessing performance. Simulating DAC designs in Simulink enables real-time visualization of system behavior, aiding in refining designs before hardware implementation.

4.4.MATLAB

MATLAB is crucial for Digital-to-Analog Converter (DAC) design, providing a comprehensive platform for modeling, simulation, and algorithm development. Its signal processing toolbox includes

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filtering, modulation, and signal generation functions, aiding efficient DAC architecture testing. MATLAB's scripting allows quick implementation and testing of custom algorithms, while its visualization tools aid real-time signal and system observation, refining DAC parameters iteratively. It emerges as an essential tool for DAC design, offering a versatile environment for algorithm development, simulation, and analysis, streamlining design across applications [8].

5. Results and Discussion

The Filter Designer app in MATLAB provides a way to simulate the filter by exporting it to SIMULINK. This provides an initial reference to check the output of the FIR filter in Libero SoC. The following are results obtained during stages of simulation.

Figure 3 Shift and Add Multiplier Output

Figure 3 is the result of behavioral simulation of a 16-bit shift and add multiplier [9]. The simulation shows how the operation starts only when the enable (en) bit is set to 1 and runs until the 'state' variable reaches 15, thereby signaling completion of the operation.

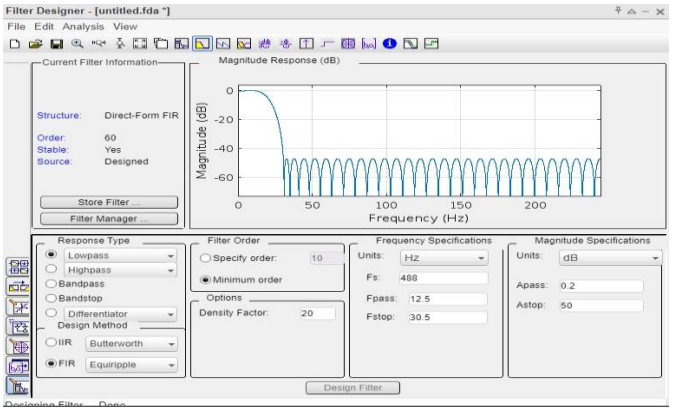

Figure 4 Output from Filter Designer App in MATLAB

The coefficients for the 60-tap filter were generated using the Filter Designer app in MATLAB and the result is shown in Figure 4.

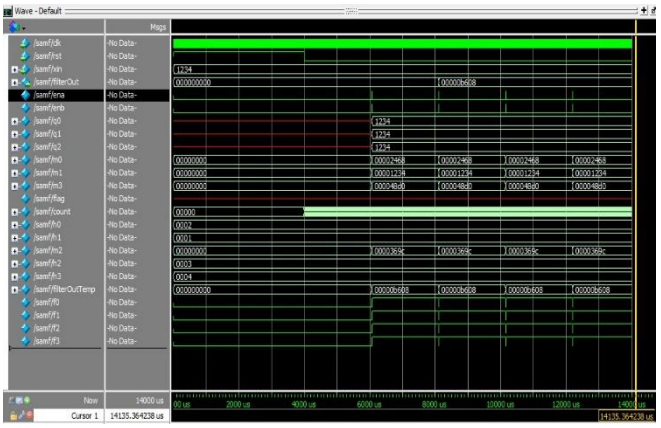

Figure 5 FIR Filter Output

Simulation result of the FIR filter in Libero SoC is shown in Figure 5 and the resources used by the filter is shown in Figure 6 [10]. The results in Figure 6 shows that the current FIR model uses comparatively less resources.

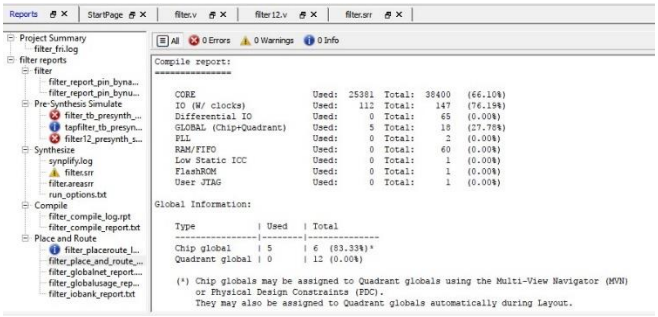

Figure 6 Resource Utilization

Conclusion

This paper addressed data acquisition system limitations by integrating an equiripple FIR filter, enhancing adaptability without physical alterations. This filter's adjustability in passband, stopband, and sampling frequencies allows for seamless reconfiguration, surpassing previous constraints. The equiripple design ensures minimal passband and stopband ripples, optimizing performance. Implementing a shift-and-add multiplier architecture reduces hardware complexity, improving efficiency. MATLAB's tools, along with SIMULINK simulations, were crucial for design verification. In

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conclusion, the project introduced a reconfigurable FIR filter, enhancing system flexibility and performance in telemetry applications, with potential for broader signal processing applications.

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