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Multi-Bit Error Resilient FPGA Cram with Minimum TTD

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Abstract

In harsh environments such as space, radiation and charged particles cause Single-Event and Multi-bit Effects, faults occurring randomly on any electronic component. These must be mitigated to ensure device functionality. Modern mitigation methods, such as triple modular redundancy, are very effective against Single Event Transients (SETs), but incur a minimum of 3× cost in area. Single-Event Upsets (SEUs) affect sequential elements and are regularly repaired using memory scrubbing. Scrubbing is a slow serial process, going through every memory word looking for errors to repair. It involves a non-negligible Time to Detect (TTD) before repair, during which other events can occur and compromise the system. Field Programmable Gate Arrays (FPGAs) rely heavily on sequential elements to store their configuration; thus, FPGA's SEU detection time is critical to ensuring design integrity in harsh conditions. It is required a robust error correction code (ECC) to protect electronic devices from MCUs. The proposed work describes the conception, implementation and evaluation of new algorithm using matrix code for the detection and correction of multiple errors in FPGA configuration memories. The combined architecture with multiple bit segment with parity bits helps in locating and correcting double-triple bit errors. The proposed Method allows asynchronous MEU detection and replaces scrubbing variable time to detect with a fixed TTD. The IMECCC based on Matrix code reduces FPGA's TTD compared to existing method.
***Keywords:** ECC (Error Code Correction); IMECCC (In-Memory Error Code Correction and Checking); MEU (Multi Event Upsets); SEU (Single Event Upsets); TTD (Time to Detect).*

1. Introduction

Field Programmable Gate Arrays are one such innovative approach that can be included in application such as satellite communication and Artificial Intelligence [1]. FPGA used in satellite communication for Signal Processing and Data Handling. In data transmission it needs dynamic resource allocation and Data detection and correction mechanisms. Data send by satellite is affected by external environmental factors such as radiation effects, extreme temperature causes the error to data. At the receiver side, Single Event Upsets (SEU) and Multi Event Upsets (MEU)will occur [2]. Scrubbing technique used to reprogram an FPGA. It is a slow serial process going through every memory word looking for errors to repair [17]. The two types of errors are hard and soft error. Hard errors are caused by physical failures, permanent and require hardware replacement in Figure 1

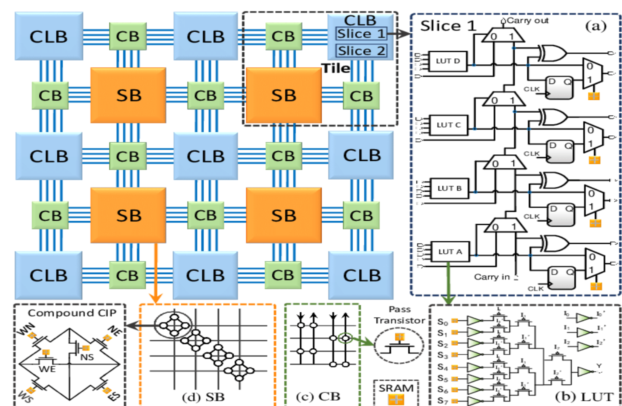

Figure 1 Internal Architecture of FPGA

While soft errors are caused by external factors usually temporary can be corrected by software. SRAM based FPGAs have a number of SRAM

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cells are called Configuration memory cells. When the configuration memory cells are hit by energy particles, the configuration bits may be flipped which is called Single Event Upsets [16]. Soft errors mitigation measures for CRAM FPGA are CRAM soft error detection function, correction function, classification function and error injection function [3-4]. The soft error detection function of the CRAM detects that an error has occurred in any one of all of the bits of the CRAM. The number of bits of the CRAM can be significant, error detection cannot be performed simultaneously for all CRAM bits, but rather is performed by scanning by each frame. The Soft error correction function automatically overwrites the detected error bit with the restoration data and restores it to its original state [5]. The occurrence of the error bit is judged whether it matches to "used" CRAM or not. With the CRAM error injection function, errors can be inserted into the actual CRAM. Related works was explained in section 2, MEU detection and correction explained in section 3, Result in section 4, Conclusion in section 5.

2. Related Works

Data transmission in advanced space communication are suffering with different kind of noises. The effect of noise in space on FPGA information can significant and include 1 [6-7]. Single Event Upsets (SEUs): High energy particles can flip individual bits in the FPGA configuration memory causing temporary errors or glitches in the operation of the device.2. Single Event Latch up (SEL): This phenomenon occurs when a high energy particle strikes the FPGA causing a temporary short circuit between the power supply rails, which can lead to latch up and damage the device.3.Total Ionizing Dose(TID):Continous exposure to ionizing radiation in space can cause cumulative damage to the FPGA, leading to degradation of performance or eventual performance over time.4.Radation induced Transient Errors: Glitches or spikes in signal lines, can occur due to radiation induced binary data transfers from one device to another device [8]. The extra parity bit applies to all the bits after Hamming code check bits have been added [9]. If one error occurs parity changes and for two errors the parity remains the same.By adding redundant bit to the Hamming code encoder it increases bandwidth and storage requirements. The Multiple bit upsets (MPU) are [11]part of error events in memory technologies. Errors are identified by low-cost error-detection code in configuration frame as well as a generic scrubbing scheme. Hamming code technique is used to detect the error in decoder [10]. It identifies errors in single, double, double adjacent errors, triple and quadruple errors with low cost. It detects two bits of error with low cost but in parity checking the permutations to detect error it occupies more space in memory cell. In [12] most common type of errors soft errors such as Single Event Upset (SEU) a change of logic state of the sequential element, Single Event Functional Interrupt (SEFI) causes functional interrupts in circuits, interfaces or entire chips and Single Event Transient (SET) a current or voltage spike in a signal. Configuration memory consists routing elements and logic resources such as Look up tables and control bits. TMR combined with scrubbing to detect and correct the errors in the configuration memory. In [13] problems caused by neutron-induced soft errors, TOF technique is used to determine the neutron velocity by measuring the flight time of the neutron along a flight path with a known length. CRAM bit error is possible at the operating frequency of the FPGA. When the circuit is operating at 250 MHZ clock, logic malfunction can be detected with in 8ns.Four techniques are used to detect the soft error of FPGA –CRAM [14], to measure high energy neutron the pulse of the accelerated particles entering the target in 1ns or less, to measure a wide En range up to hundreds of MEV, the incident neutron energy spectrum measurable within a specified precision, that neutron intensity should be high. CRAM SEU cross-sections calculated to measure logical malfunction and time distribution, number of CRAM errors and

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neutron fluence. The KHMG technology achieves a high dielectric constant by having metal for the gate. Both the gate capacitance and Critical charge increases [15]. SEU cross-sections with high resolution from 1to 800 MeV at the ICE-House of LANSCE. In [6] the behavior of FPGA under radiation to detect the error with most common method in evaluating in Single Event Effect (SEE) cross section of its elements individually. Polar Fire to assess its potential sensitivity to them. The sensitivity of Flip Flops, DSPs, and PLLs of Polar Fire was studied for protons and ThN irradiations. The cross section for the PLL proves no error as SEU with 95%accuracy, an average FF cross section 2.5x lower than its predecessor. The difference is higher DSP an average cross section of two orders of magnitude lower than its predecessor [16]. Instead of ThN, the TMR version is used. The cross section is stable with the frequency except for the WSR version in the TMR mode. The degradation of propagation delay was monitored by ring oscillator. The rings were monitored during the whole irradiation run using the tester, it shows the difference in percentage between the frequency measured before and after the irradiation [19]. Polar Fire shows high sensitivity to ThNs due to the presence of boron - 10 in the device. When two types of errors occurred, it prefers single bit error and double bit error is not corrected is the drawback.

3. Single bit error detection and correction

Errors in the code word can be detect and correct in single event upsets and Mulit-bit upset also detect in this method.SEU is commonly detected by read back bitstream scrubbing method. This method increases the Time to Detect SEU to overcome this effect scrubbing and TMR is performed to detect and correct SEU. The ECC checkers are used as sensors to detect SEU asynchronously [18]. The Combination ofHamming code with IMECCC reduce ECC failure. When two or more SEUs occur in very short period at different locations in the FPGA the affected memory words are repaired one after the other [20]. Interruption based partial reconfiguration can repair the same memory word and many times consequently in the case of many SEUs affecting this same memory word, increasing the reliability. In 32-bit data word, it is taken as 26-bit configuration data and 6 parity bits are taken to find the Single Event Upsets. In the result of this bits, if it results “00” No Error,”01” Double Bit Error,”10” Single Bit Upset on b [31]p[5],”11” SBU on b[ECC[MSB-1:0]-1]. Hamming based reconfiguration and the cost of double error detection which requires system intervention to repair the affected memory word. Therefore, this technique has been designe.to detect SEUs faster than read back-scrubbing to minimize the time to detect the SEUs.

3.1. IMECCC Multi-Bit Error Detection and Correction

In FPGA, bit stream is feed in the kit with parity bits. Matrix code method is proposed to generate parity bits. Multi-Bit Upsets can be detected and correct with minimum TTD [21].

3.2. Proposed Method

Figure 2 depicts the block diagram of the proposed system [22]. Such detection times are systems liability and limit the utilization of FPGAs for critical applications. A new FPGA architecture and design methodology to replace bitstream scrubbing with asynchronous SEU detection to reduce systems’ liability is proposed. A main contribution of the proposed work is multi-bit error correction using matrix codes and detection time improvements [23].

3.3. Error Correction Based on Matrix Codes

The proposed detection/correction scheme is called Matrix codes (MC) since the protection’s bits are used in a matrix format. In this case, the n-bits code word is divided into k1 numbers words of width k2. A (k1, k2) matrix is formed where k1 and k2 represent numbers of rows and columns. For each of the k1 rows, the check bits are added for single error correction/double error detection. Another k2 bits are added as vertical parity bits. We explain the basic technique by considering a 16-bit word length memory.

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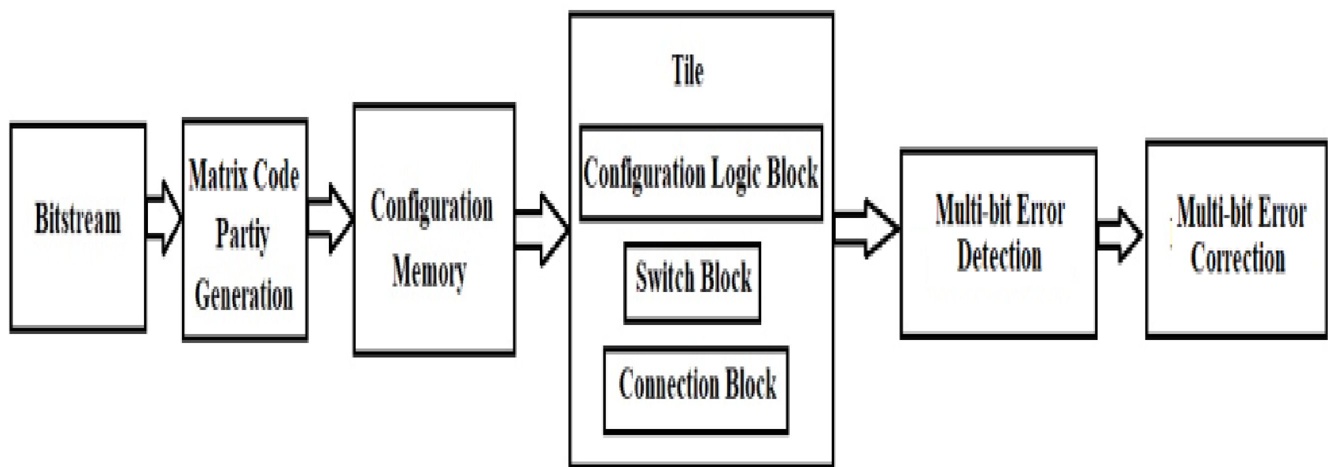

Figure 2 **Block Diagram of Proposed Method**

X_1	X_2	X_3	X_4	C_1	C_2	C_3
X_5	X_6	X_7	X_8	C_4	C_5	C_6
X_9	X_{10}	X_{11}	X_{12}	C_7	C_8	C_9
X_{13}	X_{14}	X_{15}	X_{16}	C_{10}	C_{11}	C_{12}
P_1	P_2	P_3	P_4			

Figure 3 **A 16-Bit Data Word with Check Bits and Parity Bits**

A Hamming decoder is used to decode each row. Decoding is done in two steps. First, the horizontal check bits are calculated using the saved data bits and compared with the saved horizontal check bits [24]. This procedure is called syndrome bit generation and is called syndrome bit of check bit. Second, using syndrome bits, the single error detection (SED)/double error detection (DED)/no error (NE) signals are generated for each row. If DED is activated (double error is detected in a row), we use the vertical syndrome bits and the saved value of the bit we can correct any single or double erroneous bits in each row. It is important to mention that if more than two errors are present in the code word, MCs can correct two errors in any row assuming that we have only one error in other rows. If only two errors occur, then these can be corrected without any restriction. Algorithm 1 MATRIX code verification algorithm (X: data)

- Read the saved data bits of X
- Generate check bits using saved data bits (C0-C19)
- Generate syndrome bits of check bits (SC0-SC19)
- Generate parity bits using saved data bits (P0-P7)
- Generate syndrome bits of parity bits (SP1-SP7)
- Correct every saved bit if it is error
- Output the corrected word

Algorithm 1 shows the procedure of detection and correction in the proposed Matrix method which is applied on a code word, where and are the check bits and the parity bits that are calculated using the saved data bits in the memory [25]. These are then compared with saved in memory check bits and parity bits to calculate the syndrome bits SC and SP in Figure 3.

4. Result and Discussion

4.1. Simulation Result of LUT

Simulation is programmed to implement an inverter whose LUT output (0) is always an inversion of its first input (A1). Other inputs A2, A3, and A4 act as “don’t-care” bits but their values affect the signal propagation path from A1 to the output (0) in Figure 4 & 5.

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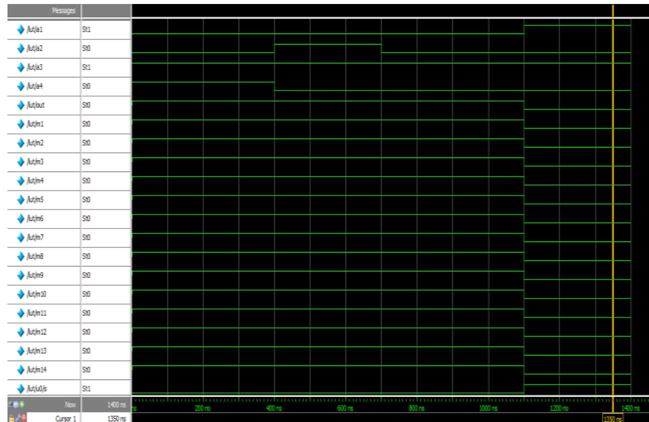

Figure 4 **Simulation Result of LUT**

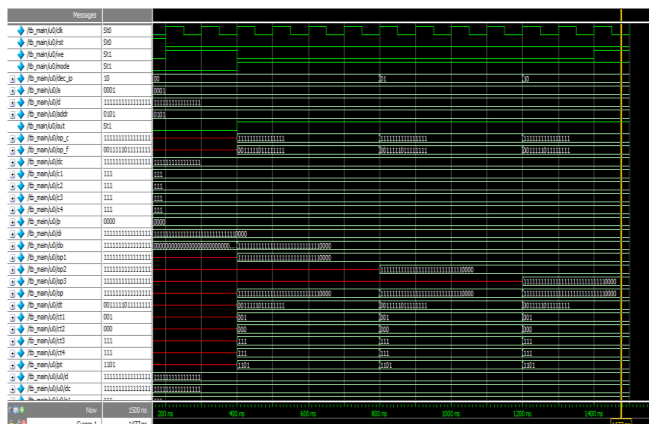

Figure 5 **Simulation Result of IMECCC MEU Error Detection and Correction**

The signal propagation path from A1 to the output (0) is shortest for A2A3A4 = 000 and longest for A2A3A4 = 111 for 4-input LUT's. Thus, a programmable delay inverter with three control inputs can be implemented by using one LUT. For the PDL, the first LUT input A1 is the inverter input and the rest of the LUT inputs (three) are controlled by 2 3 = 8 discrete level. CLK and RST are the input signals. The input MODE is used for selecting programming phase and operating phase. DEC_IP is used for selecting CLB, SB and CB in a tile. D is the bitstream data to be stored in CRAM. DI is the parity added hamming code data of the input. OP1(OP1_F), OP2(OP2_F) and OP3(OP3_F) are the output(faulty) value of CLB, SB and CB, respectively.C1-C4 and P is the parity bits of matrix codes.OP_F shows fault in three bits.All the three faults is detected and corrected by proposed method and output is obtained in OP_C shown in Table 1 Figure 6.

Table 1 **Comparison of Single Bit and Multi Bit Error**

S. No	1	2	3	4	5	6	7
rms							
SEU							
IMEU							

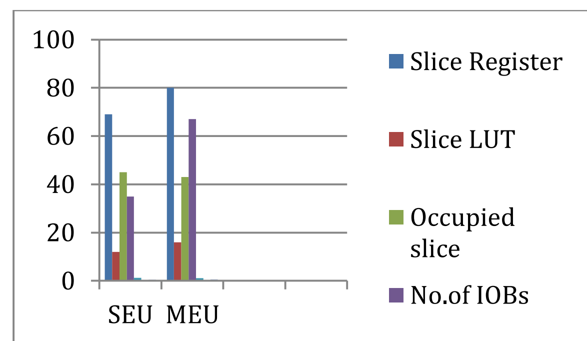

Figure 6 **Comparison of Single Bit and Multi Bit Error**

Conclusion

A built-in solution to detect MBU in FPGAs' configuration memory asynchronously called IMECCC is proposed. It is a new FPGA architecture using multi-bit correction built from ECC checkers as an alternative to bit stream scrubbing to quickly and asynchronously detect bit-flip in FPGA CRAM. A high-level error detection and correction method using matrix code is used. The proposed protection code combines Hamming code and Parity code, so that multiple errors can be detected and corrected. The fault-injection based experimental results show that the proposed Matrix method provides good detection and correction coverage. This detection method demonstrates an improvement of TTD reduction compared to the MTTD for read-back scrubbing. Such significant results are made possible by replacing the serial process from the state-of-the-art scrubbing method with the IMECCC. Furthermore, our solution uses a

specific floor plan pattern, which, along with the CLB design, shows the capability to reinforce integrated ECC codes. Despite the cost in area induced by the ECC integration, the IMECCC solution provides better solutions compared to stateof-the-art SEU mitigation methods for FPGAs.

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