International Research Journal on Advanced Engineering Hub (IRJAEH)
e ISSN: 2584-2137
Vol. 04 Issue: 06 June 2026
Page No: 4382 - 4386
https://irjaeh.com
https://doi.org/10.47392/IRJAEH.2026.0571

VLSI Implementation of Energy-Efficient Approximate ALU

Dr.Tamilselvi P[1], Jeyasudha S[2], Ranjitha R[3], Sanmugapriya M[4], Neethu K[5], Mahesh sharmila R[6]
[1]Associate professor, Department of M.E VLSI Design, Sree Sakthi Engineering College, Coimbatore, Tamil Nadu, India.
[2,3,4,5,6]PG Scholar, Department of M.E VLSI Design, Sree Sakthi Engineering College, Coimbatore, Tamil Nadu, India.
Emails: *dr.tamilselvip2024@gmail.com[1], sivasakthisudha31@gmail.com[2], deepikaranjitha381@gmail.com[3] sanmugapriyatamilarasan@gmail.com[4], kneethu210@gmail.com[5], mahesharmila@gmail.com[6]*

Abstract
Approximate Arithmetic Logic Unit (ALU) design has emerged as a promising approach for enhancing energy efficiency in modern computing systems, particularly in error-tolerant applications such as multimedia processing, machine learning, and signal processing. By intentionally relaxing computational accuracy, approximate ALUs reduce circuit complexity, switching activity, and critical path delay, thereby achieving significant improvements in power consumption and performance. This work presents a technical overview of approximate ALU architectures, focusing on techniques such as truncated computation, speculative addition, and logic simplification. Various approximation strategies are analysed in terms of error metrics, including mean error distance (MED) and error rate, alongside hardware metrics such as area, delay, and energy consumption. The trade-offs between accuracy and efficiency are explored to identify optimal design configurations for specific application domains. Simulation results demonstrate that approximate ALUs can achieve substantial energy savings with minimal impact on output quality, making them suitable for energy-constrained environments like embedded systems and IoT devices. The study concludes that approximate computing is a viable paradigm for next-generation low-power digital design.
Keywords: *Approximate Computing, ALU Design, Energy Efficiency, Error-Tolerant Systems, Low Power Design, Digital Circuits, IoT, Hardware Optimization, Speculative Adders, Truncated Arithmetic.*

1. Introduction
The rapid advancement of data-intensive applications and portable electronic devices has created a strong demand for energy-efficient computing systems. Arithmetic Logic Units (ALUs), which serve as the core computational blocks of processors, are conventionally designed to perform exact operations with high precision. Although accurate, these exact ALUs often consume considerable power, occupy larger chip area, and introduce higher delay. Modern applications such as image processing, multimedia systems, machine learning, and IoT-based devices can tolerate small computational errors without noticeably affecting the final output. This characteristic has encouraged the development of approximate computing as an effective low-power design approach. Approximate ALUs intentionally allow limited inaccuracies in arithmetic and logical computations to improve hardware efficiency. By reducing circuit complexity, minimizing transistor usage, and lowering switching activity, these ALUs achieve significant reductions in power consumption and computation time. Several approximation methods, including truncated arithmetic, speculative computation, voltage over-scaling, and approximate logic synthesis, are widely adopted to optimize performance while maintaining acceptable accuracy levels [1].

2. Literature Review
In recent years, the demand for low-power and high-speed digital systems has increased rapidly due to the

growth of portable devices, IoT systems, artificial intelligence, and multimedia applications. Conventional Arithmetic Logic Units (ALUs) consume significant power because they perform fully accurate computations. To overcome this limitation, researchers introduced the concept of approximate computing, where small computational errors are tolerated to achieve improvements in power consumption, speed, and chip area. Early research in approximate arithmetic mainly focused on approximate adders and multipliers, which are the fundamental building blocks of ALUs. Studies showed that reducing carry propagation in adders significantly decreases power dissipation and delay. Researchers proposed error-tolerant adders and multi-bit approximate adders that achieved better trade-offs between accuracy and energy efficiency compared to conventional exact adders. Several researchers developed energy-efficient approximate full adders using CMOS and Fin FET technologies. These designs reduced transistor count, switching activity, and leakage power while maintaining acceptable computational accuracy. Experimental results demonstrated considerable reductions in dynamic power and propagation delay, making approximate ALUs suitable for error resilient applications such as image processing, machine learning, and signal processing. Comparative studies on approximate adders analysed parameters such as power consumption, area utilization, delay, and error metrics. These studies classified approximate adders into FPGA-based and ASIC-based implementations and concluded that approximate arithmetic circuits provide better Area Delay Product (ADP) and energy savings than accurate arithmetic units. Survey papers on approximate arithmetic circuits highlighted the importance of approximation techniques in modern VLSI systems. Researchers explained that approximate ALUs can improve overall processor efficiency by sacrificing a small amount of computational accuracy. These techniques are especially beneficial in applications where exact outputs are not mandatory. Recent VLSI research also combines approximate ALU architecture with low-power optimization methods such as clock gating, power gating, voltage scaling, and transistor-level optimization. These methods further reduce static and dynamic power consumption in integrated-circuits [2].

3. Proposed Methodology

The proposed system focuses on designing and implementing an energy-efficient Approximate Arithmetic Logic Unit (ALU) using VLSI technology. The objective is to reduce power consumption, propagation delay, and chip area while maintaining acceptable computational accuracy for error-tolerant applications. Initially, the ALU architecture is designed by integrating approximate arithmetic circuits such as approximate adders and approximate multipliers. Approximation techniques are applied mainly in the least significant bits (LSBs) to reduce switching activity and hardware complexity without significantly affecting overall output quality. The proposed ALU consists of arithmetic operations such as addition, subtraction, multiplication, and logical operations including AND, OR, XOR, and NOT. Approximate full adders are implemented to minimize transistor count and reduce dynamic power dissipation. The circuit design and simulation are carried out using HDL languages such as Verilog/VHDL. The designed modules are synthesized using VLSI design tools to evaluate parameters including: To improve energy efficiency further, low-power techniques such as clock gating, voltage scaling, and optimized transistor sizing are incorporated into the design. Functional verification is performed using simulation waveforms and test benches. Finally, the performance of the proposed approximate ALU is compared with a conventional exact ALU. The comparison is based on power, speed, area, and accuracy metrics. The expected outcome is a low-power and high-speed ALU suitable for applications such as image processing, multimedia systems, AI accelerators, and embedded devices where minor computational errors are acceptable [3].

4. System Architecture

The architecture of an approximate Arithmetic Logic Unit (ALU) is developed to achieve a balance between computational performance and tolerable error levels, making it highly appropriate for low-power applications. This architecture generally includes modular functional blocks such as approximate adders, subtractors, multipliers, and

International Research Journal on Advanced Engineering Hub (IRJAEH)
e ISSN: 2584-2137
Vol. 04 Issue: 06 June 2026
Page No: 4382 - 4386
https://irjaeh.com
https://doi.org/10.47392/IRJAEH.2026.0571

logic circuits connected through a configurable control unit. Each functional module is optimized using approximation methods to decrease power usage, hardware complexity, and computation delay. Within the architecture, approximate adders are considered one of the most important components because addition operations occur frequently in digital processing systems. These adders commonly apply methods like carry truncation, speculative carry prediction, and segmented processing to reduce switching activity and improve efficiency. In the same way, approximate multipliers adopt techniques such as partial product reduction and simplified accumulation mechanisms to lower energy consumption. Logical operations including AND, OR, and XOR can also be realized using compact transistor-level implementations or probabilistic logic circuits. An essential feature of the architecture is the accuracy management unit, which controls the approximation level according to the application's requirements. This is generally implemented through configurable operating modes that allow switching between exact and approximate computation. Furthermore, error detection or monitoring units may be integrated to evaluate deviation parameters and ensure that the produced output remains within permissible quality limits. To further improve power efficiency, the architecture is often combined with low-power clocking strategies and voltage scaling methods. Its compatibility with processor pipeline structures enables efficient integration into embedded systems and Internet of Things (IoT) applications. Overall, the approximate ALU architecture offers a flexible and scalable solution that effectively balances computational accuracy with reduced energy consumption [4].

5. Block Diagram

The proposed block diagram illustrates the architecture of an energy-efficient Approximate Arithmetic Logic Unit (ALU) designed using VLSI technology. The primary objective of this architecture is to minimize power consumption, propagation delay, and hardware complexity while maintaining a satisfactory level of computational accuracy. The Control Unit functions as the main supervisory block of the ALU. It receives opcode and mode selection inputs and decides which arithmetic or logical operation must be executed. Depending on the control signals, the corresponding functional module is enabled for operation [5]. The Approximate Addition block carries out addition operations using approximate adder circuits Shown in Figure 1.

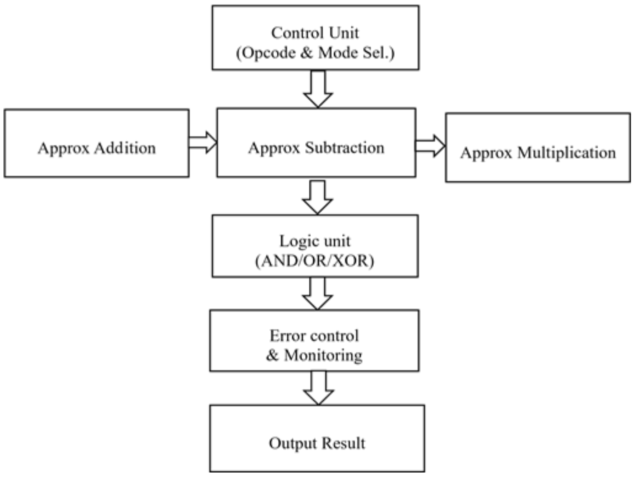

Figure 1 Block Diagram of Approximate ALU

These adders intentionally allow minor inaccuracies to reduce switching activity and transistor utilization, resulting in improved power efficiency and faster computation. In a similar manner, the Approximate Subtraction block performs subtraction operations with minimized carry or borrow propagation, thereby reducing delay and energy consumption. The Approximate Multiplication block executes multiplication operations using a simplified multiplier structure. Since multiplication generally requires large hardware resources and higher power, approximation methods significantly decrease chip area and power dissipation while maintaining acceptable output quality. The Logic Unit is responsible for performing fundamental logical operations such as AND, OR, and XOR, which are widely used in digital processing applications. An Error Control and Monitoring block is included to observe the accuracy of approximate outputs and ensure that the generated errors remain within permissible limits. Finally, the processed data is transferred to the Output block. Overall, the proposed approximate ALU achieves low-power, area-efficient, and high-speed performance, making it highly suitable for modern applications including

International Research Journal on Advanced Engineering Hub (IRJAEH)
e ISSN: 2584-2137
Vol. 04 Issue: 06 June 2026
Page No: 4382 - 4386
https://irjaeh.com
https://doi.org/10.47392/IRJAEH.2026.0571

multimedia processing, artificial intelligence, embedded systems, IoT devices, and image-processing systems [6].

6. Results and Discussion

The proposed Approximate ALU was developed and simulated using HDL programming and standard VLSI design tools to evaluate its hardware performance. The system performance was examined using important parameters such as power consumption, propagation delay, chip area, and computational accuracy. The obtained outcomes were compared with those of a traditional exact ALU architecture. Simulation analysis indicated that the approximate ALU achieved considerable power reduction because of simplified arithmetic circuits and optimized logic structures. The decrease in switching activity and transistor utilization significantly minimized dynamic power dissipation within the circuit. The propagation delay of the proposed design was also improved, as approximation methods reduced carry propagation during arithmetic operations. Approximate addition and subtraction modules provided faster computation compared to accurate arithmetic circuits. In addition, the approximate multiplication unit occupied smaller silicon area and consumed less power while maintaining acceptable output quality for error-resilient applications. Logical operations including AND, OR, and XOR were implemented successfully with reliable and stable functionality. An Error Control and Monitoring unit was incorporated to ensure that the generated errors remained within permissible limits. Although minor inaccuracies were present in computation, they did not noticeably affect the performance of multimedia, image processing, and signal-processing applications where exact precision is not essential. Comparative evaluation proved that the proposed ALU achieved a better Power Delay Product (PDP) and enhanced hardware efficiency than conventional ALU designs. Thus, the developed energy-efficient approximate ALU is highly suitable for low-power applications such as embedded systems, artificial intelligence, portable electronics, and IoT devices requiring reduced power consumption with high-speed operation Shown in Figure 2 Graphical Representation of Approximate ALU [7 - 9].

7. Output Implementation Image

Time (ns)	Mode (Binary)	Operation	A (8-bit)	B (8-bit)	Approx En	RESULT(Hex)	CARRY OUT	ZERO
20	000	ADD	15	27	1	002A	0	0
100	001	SUB	15	27	1	FFF3	1	0
180	010	MUL	15	27	1	011D	0	0
260	011	AND	15	27	1	0036	0	0
340	100	XOR	15	27	1	0000	0	1

Figure 2 Graphical Representation of Approximate ALU

Conclusion

In this project, an energy-efficient Approximate Arithmetic Logic Unit (ALU) was successfully designed and implemented using VLSI technology. The proposed architecture utilized approximate computing techniques to reduce power consumption, propagation delay, and hardware complexity while maintaining acceptable computational accuracy. The implementation of approximate adders, subtractors, and multipliers helped in minimizing transistor count and switching activity, which significantly improved overall energy efficiency. Simulation and performance analysis showed that the proposed approximate ALU achieved lower power dissipation and faster operation compared to conventional exact ALU designs. Although minor computational errors were introduced, the error level remained within acceptable limits for error-tolerant applications such as image processing, multimedia systems, artificial intelligence, and embedded devices. The Error Control and Monitoring unit further improved the reliability of the system by ensuring controlled approximation. The comparative analysis confirmed that the proposed design provides better Power Delay Product (PDP), reduced area utilization, and enhanced hardware efficiency. Thus, the proposed VLSI implementation of an energy-efficient approximate ALU offers an effective solution for modern low-power digital systems. In future work, the design can be extended using advanced CMOS technologies, FPGA implementation, and adaptive approximation techniques to achieve even better performance and energy optimization for next-generation computing applications.

References

[1]. Xiang Fei, Optimized Design and Applications of Arithmetic Logic Units: Addressing Power Efficiency and Performance in Diverse Computing Applications, Proceedings of the 5th International Conference on Materials Chemistry and Environmental Engineering DOI: 10.54254/2755-2721/128/2025.20216
[2]. Nykolaychuk Y, Hryha V, Vozna N, et al. High-performance coprocessors for arithmetic and logic operations of multi-bit cores for vector and scalar supercomputers. 2022 12th International Conference on Advanced Computer Information Technologies (ACIT). IEEE, 2022: 410-414.
[3]. Chen M, Ma X, Xu B. A Design of ALU Comparator for High Performance RISC-V Processor. InternationalConference on Internet of Things, Communication and Intelligent Technology. Singapore: Springer Nature Singapore, 2022: 351-357.
[4]. Sengupta S, Sarkar P, Dastidar A. Design of a 4 Bit Arithmetic & Logic Unit, Evaluation of Its Performance Metrics & its Implementation in a Processor. 2020 International Conference for Emerging Technology (INCET). IEEE,2020: 1-8.
[5]. Mirzaei M, Mohammadi S. Low-power and variation-aware approximate arithmetic units for image processing applications.
[6]. AEU-International Journal of Electronics and Communications, 2021, 138: 153825.
[7]. Tang G M, Qu P Y, Ye X C, et al. Logic design of a 16-bit bit-slice arithmetic logic unit for 32-/64-bit RSFQ microprocessors. IEEE Transactions on Applied Superconductivity, 2018, 28(4): 1-5.
[8]. Joshi R, Parekh R, Agrawal Y. Design and optimization of single electron transistor based 4-bit arithmetic and logic unit at room temperature operation. 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS). IEEE, 2017: 34-39.
[9]. Kamaraj A, Marichamy P. Design and implementation of arithmetic and logic unit (ALU) using novel reversible gates in quantum cellular automata. 2017 4th International Conference on Advanced Computing and Communication Systems (ICACCS). IEEE, 2017: 1-8