International Research Journal on Advanced Engineering Hub (IRJAEH)
e ISSN: 2584-2137
Vol. 04 Issue: 05 May 2026
Page No: 3686-3688
https://irjaeh.com
https://doi.org/10.47392/IRJAEH.2026.0481

Review of Vedic Multiplier Architectures for High Performance FFT Processing

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Abstract

One of the basic arithmetic operations in digital systems is multiplication, especially in applications such as spectral analysis, image processing, and signal processing. Multiplier performance directly impacts factors like speed, power efficiency, and system throughput. Traditional architectures such as array multipliers, Wallace tree multipliers, and Booth multipliers improve either speed or area efficiency but fail to optimize both simultaneously.Vedic mathematics offers an alternative approach through sutra-based computational techniques such as Urdhva-Tiryakbhyam and Nikhilam, which enable high parallelism, reduced propagation delay, and modular scalability. This review paper consolidates research on 16-bit Vedic multiplier designs and analyzes their integration in FFT (Fast Fourier Transform) processors. It examines conventional, modified, and hybrid Booth–Vedic architectures implemented on FPGA and ASIC platforms. Comparative results show that hybrid Booth–Vedic designs achieve up to 89% reduction in area and 72% improvement in Area–Delay Product (ADP) compared to conventional designs. The paper also discusses architectural trade-offs, implementation challenges, and future research directions for advancing Vedic arithmetic hardware in next-generation digital systems.

Keywords: *Booth–Vedic architecture; FFT processor; FPGA; Low power design; Vedic multiplier*

1. Introduction

The computational foundation of most Digital Signal Processing (DSP) systems is multiplication, which is widely used in convolution, neural network computations, filtering, and Fourier transforms. Since each butterfly computation in the Fast Fourier Transform (FFT) requires multiple complex multiplications, FFT processors are highly dependent on high-speed multipliers. Therefore, optimizing multiplier design can significantly improve the throughput and energy efficiency of FFT systems.

Despite their effectiveness, conventional multiplier designs exhibit certain trade-offs. For instance, array multipliers have a simple structure but operate slowly due to long critical paths. Booth multipliers reduce the number of partial products but introduce complexity through encoding and decoding processes. Wallace tree multipliers offer higher speed but at the cost of increased power consumption and silicon area. Vedic multipliers, derived from ancient Indian mathematics, provide a balanced solution. Using sutra-based computation techniques such as Urdhva-Tiryakbhyam and Nikhilam, they enable parallel generation of partial products, reduced propagation delay, and modular scalability. This modularity allows designs to scale from smaller bit-widths such as 4×4 to larger configurations like 16×16 without altering the fundamental architecture, making them well-suited for FPGA-based implementations and FFT processor designs. Vedic mathematics consists of sixteen sutras that define efficient computational methods. Among these, Urdhva-Tiryakbhyam (“vertically and crosswise”) and Nikhilam Navatascaramam Dashatah (“all from 9 and the last from 10”) are particularly significant in digital multiplier design. The Urdhva-Tiryakbhyam algorithm enables parallel generation of partial products, significantly reducing propagation delay compared to conventional sequential methods. On the other hand, the Nikhilam technique simplifies multiplication when numbers are close to a power of two by reducing hardware complexity through simple addition and subtraction operationsA 16-bit Vedic multiplier can be constructed hierarchically using smaller 4×4 or 8×8 modules based on the Urdhva-Tiryakbhyam method. This hierarchical approach enhances modularity, promotes design reuse, and ensures efficient utilization of FPGA resources. As a result, it provides a regular layout, shorter critical paths, and improved scalability, which are essential for high-performance DSP systems such as FFT processors [1-5].

2. Method

The proposed approach focuses on the design and analysis of Vedic multiplier architectures and their integration into FFT processors. The methodology is based on implementing Vedic multiplication techniques, particularly the Urdhva-Tiryakbhyam (UT) sutra, to achieve high-speed and area-efficient computation. The UT algorithm enables parallel generation of partial products, significantly reducing propagation delays compared to conventional sequential multiplication methods. A hierarchical design approach is adopted, where a 16×16 Vedic multiplier is constructed using smaller 4×4 and 8×8 multiplier modules. These modules are combined using efficient adder structures such as carry-save adders and ripple-carry adders to produce the final output. This modular structure ensures scalability, design reuse, and efficient utilization of FPGA resources. To enhance performance, hybrid architectures combining Booth encoding with Vedic multiplication are also considered. Booth encoding reduces the number of partial products, while Vedic techniques ensure parallel processing, resulting in improved speed and reduced area. These architectures are implemented and analyzed on FPGA and ASIC platforms to evaluate parameters such as delay, area utilization, and power consumption. The methodology also includes integrating the designed multipliers into FFT processors, where they are used in butterfly computation units. This integration enables faster computation of twiddle factors and improves overall system throughput. Performance evaluation is carried out by comparing conventional, modified, and hybrid multiplier designs in terms of speed, power efficiency, and Area–Delay Product (ADP).

3. Results and Discussion

3.1. Results

A comparison of existing studies on Vedic multipliers shows a clear trend toward increased speed, reduced area, and improved power efficiency. The conventional 16×16 Vedic multiplier proposed by Bansal et al. (2015) demonstrated a 20% increase in speed and a 15% reduction in silicon area compared to Booth multipliers, establishing a strong foundation for Vedic-based designs. Similarly, Gejji et al. (2015) validated the application of Vedic techniques in real-time digital signal processing by integrating Vedic arithmetic into FFT processors, resulting in reduced computational delay and lower hardware complexity [6-10]. Further improvements were introduced by Gaur et al. (2019), who focused on enhancing power efficiency using hybrid adder structures such as multiplexed sum and Brent-Kung adders. Their design achieved a 59% reduction in power consumption and a 46% improvement in performance due to reduced combinational delay. More recently, Kalaiselvi and Sabeenian (2023) proposed a hybrid Booth–Vedic architecture that combines Booth encoding with Vedic multiplication. This design achieved up to 89% reduction in area and 72% improvement in Area–Delay Product (ADP) on FPGA platforms, demonstrating significant advancements in both performance and efficiency.

3.2. Discussion

The results indicate that Vedic multiplier architectures outperform conventional multipliers in terms of speed due to their inherent parallelism. However, hybrid architectures that combine Vedic methods with techniques such as Booth encoding provide a more balanced trade-off between speed, power consumption, and hardware utilization. These designs address key limitations of traditional Vedic multipliers, such as handling signed operations and improving scalability. Despite these advancements, several challenges remain. As bit-width increases beyond 32 bits, carry propagation delay becomes significant, requiring the use of advanced adder structures such as carry look-ahead and carry-save adders. Additionally, traditional Vedic algorithms are primarily optimized for unsigned arithmetic, making their extension to signed and floating-point operations more complex. Hardware routing complexity is another critical issue in large FPGA implementations due to interconnect congestion. Furthermore, the lack of pipelining and compression techniques limits scalability at higher word lengths. Future research can focus on integrating compressor adders such as 4:2 and 7:2 compressors to improve parallel reduction of partial products. Techniques such as low-power synthesis and dynamic clock gating can further enhance energy efficiency. The application of Vedic multipliers in AI accelerators and real-time FFT systems also presents promising opportunities for future development. Additionally, approximate Vedic arithmetic can be explored for applications that can tolerate minor computational errors, such as image processing and neural computing.

Conclusion

Vedic multipliers based on the Urdhva-Tiryakbhyam sutra provide significant improvement in digital arithmetic design by achieving high speed, low power consumption, and modular scalability. Their inherent parallelism and hierarchical structure make them highly suitable for integration in FFT and DSP processors. Recent advancements, particularly hybrid Booth–Vedic architectures, effectively balance speed, area, and power, overcoming limitations of conventional multipliers. These developments confirm that Vedic multiplier architectures are a strong alternative for high-performance digital systems. With ongoing improvements in hybrid design techniques, pipelining, and reconfigurable logic, Vedic multipliers are expected to play a crucial role in next-generation applications such as embedded DSP systems, AI accelerators, and low-power edge computing devices.

Acknowledgements

The authors would like to express their sincere gratitude to Dayananda Sagar College of Engineering for providing the necessary support and resources to carry out this work. The authors also thank the faculty members of the Electronics and Telecommunication Engineering department for their guidance and encouragement throughout the research.

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