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Development of Fault Tolerant Digital System Using Triple Modular Redundancy

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Abstract

Urban buildings use a large amount of electrical energy every day, especially for cooling. One common reason Fault tolerance is a critical requirement in safety-critical and high-reliability digital systems such as aerospace electronics, medical devices, industrial automation, and communication infrastructure. This project focuses on the design and development of a fault-tolerant digital system using the Triple Modular Redundancy (TMR) technique [1], [3]. In a TMR architecture, three identical modules execute the same operation in parallel, and a majority voting mechanism determines the correct output even if one module fails due to transient faults, permanent hardware failures, or radiation-induced errors [1]. The proposed system implements replication at the hardware level and incorporates a robust majority voter circuit to ensure continuous operation without performance degradation [2], [3]. The design is simulated and validated using digital design tools to analyze system behavior under fault-injection scenarios. Performance metrics such as reliability, error-masking capability, propagation delay, and resource utilization are examined to evaluate the effectiveness of the TMR approach. The results demonstrate that TMR significantly enhances system reliability and resilience by masking single-point failures, making it a practical solution for mission-critical applications where system downtime or incorrect outputs are unacceptable [1], [3]. This project provides a comprehensive understanding of fault-tolerant design strategies and highlights the trade-offs between hardware redundancy, system complexity, and operational reliability.

Keywords: *Error detection and correction; Fault -tolerant digital system; Hardware redundancy; Majority voter / voting logic; Reliability and availability; Triple Modular Redundancy (TMR).*

1. Introduction

Modern digital systems are increasingly deployed in environments where continuous and correct operation is crucial, such as aerospace, medical equipment, industrial automation, and defense applications. In these domains, even a single fault can lead to system failure, financial loss, or threats to human safety. Faults may arise from transient effects like radiation-induced single event upsets, as well as permanent failures caused by manufacturing defects, aging, or harsh operating conditions. As integrated circuits become more complex and transistor sizes shrink, the susceptibility of digital hardware to such faults continues to grow, making fault tolerance a key design requirement for modern electronic systems [1]. To address these challenges, hardware redundancy techniques have emerged as effective solutions for improving system reliability and availability. Among these techniques, Triple Modular Redundancy (TMR) is one of the most widely used and practical approaches for fault-tolerant design. In TMR, three identical copies of a critical module operate in parallel on the same inputs, and a majority voter circuit determines the final output based on the consensus of these modules. If one of the modules fails or produces an erroneous result, the other two correct outputs

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outvote the faulty one, allowing the system to continue functioning correctly without interruption [1], [3]. This principle makes TMR particularly attractive for safety-critical and real-time applications where system downtime or incorrect operation is unacceptable. This project focuses on the development of a fault-tolerant digital system using **Triple Modular Redundancy** as the core design methodology. The work involves designing triplicated logic blocks, implementing an efficient majority voter, and integrating these components into a complete digital system architecture. The design is targeted for implementation on a programmable hardware platform such as a **microcontroller**, enabling experimentation with fault injection and evaluation of system behavior under various fault conditions [2], [3]. Through analysis of resource usage, timing performance, and fault-masking capability, the project aims to demonstrate that TMR can significantly enhance system reliability with acceptable hardware overhead, making it a practical design strategy for robust digital systems in critical applications.

1.1. Method of Sign Language

This methodology section outlines the main stages for designing and validating a fault-tolerant digital system using Triple Modular Redundancy (TMR). It is written in a general way so you can adapt it to your specific hardware and tools.

2. System Design Overview

The methodology begins with the specification of the target digital function and its fault-tolerance requirements, followed by the design of a TMR architecture and its implementation on a suitable hardware platform. Each step focuses on ensuring that the system can continue correct operation in the presence of single-module faults and can be practically realized with acceptable resource and timing overhead.

2.1. Step 1: Problem Definition

Identify the target digital subsystem (e.g., ALU, controller, encoder, or specific logic block) that must be made fault tolerant, and define its functional inputs, outputs, and timing constraints. Specify the fault model to be considered, such as transient single event upsets (SEUs), stuck-at faults, or permanent logic failures, and determine the acceptable fault coverage and performance trade-offs for the application domain (e.g., aerospace, industrial control).

2.2. Step 2: Base Module Design

Design and simulate a single, non-redundant version of the digital module using HDL (VHDL/Verilog) or an equivalent design flow, ensuring it meets functional requirements and timing constraints. Verify the base module through functional simulation and test benches, so that any erroneous behaviour observed later during TMR evaluation can be attributed to faults and not to design errors.

2.3. Step 3: TMR Architecture Development

Create a TMR architecture by instantiating three identical copies of the verified base module and connecting all three to the same input signals, keeping the internal logic of each replica identical.
Design a majority voter circuit for each output (or output bus) of the module, implementing bitwise majority logic so that the final system output is determined by at least two matching module outputs.

2.4. Step 4: Integration and HDL Implementation

Integrate the triplicated modules and their associated majority voter(s) into a top-level HDL design, ensuring proper signal naming, clock distribution, and reset handling for all three modules. Apply design constraints (timing, pin assignments, clock frequencies) appropriate for the chosen hardware platform, such as a specific Micro controller development board or custom digital system.

2.5. Step 5: Synthesis and Hardware Mapping

Synthesize the TMR design using standard EDA tools to map the HDL description into gate-level or Micro controller resource-level implementations, and record metrics such as logic utilization, flip-flop count, and on-chip routing. Perform static timing analysis to ensure that inclusion of triplicated logic and voter circuits does not violate critical-path timing or system clock requirements.

2.6. Step 6: Functional Verification of TMR System

Run functional simulations of the complete TMR system under normal operating conditions (no injected faults) to confirm that it produces identical

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outputs to the original single-module design for the same test vectors. Use comprehensive test benches that cover typical and corner-case input scenarios so that the TMR structure is validated not only structurally but also behaviourally.

2.7. Step 7: Fault Injection and Robustness Testing

Introduce controlled faults into one of the three module instances in simulation (e.g., forcing signals, flipping bits in registers, or modelling stuck-at faults) to emulate transient or permanent failures. Observe the majority voter outputs and verify that the TMR system masks single-module faults, maintaining correct overall output as long as at most one replica (Table 1).

Table 1 Fault Analysis Output (TMR)

Fault Case	M1	M2	M3	Output	Status
No fault	✓	✓	✓	Correct	Normal
Fault in M1	✗	✓	✓	Correct	Tolerated
Fault in M2	✓	✗	✓	Correct	Tolerated
Fault in M3	✓	✓	✗	Correct	Tolerated
Fault in M1&M2	✗	✗	✓	Wrong	Failure
Fault in M2&M3	✓	✗	✗	Wrong	Failure
Fault in M1&M3	✗	✓	✗	Wrong	Failure

3. Result and Discussion

3.1. Result

The result of implementing a fault-tolerant digital system using Triple Modular Redundancy (TMR) in microcontroller components demonstrates a substantial improvement in reliability and system robustness. The microcontroller continues to operate correctly even when one of the replicated components experiences a fault, as the majority voter consistently selects the correct output. This fault-masking capability ensures uninterrupted operation and prevents system failure in critical conditions. Additionally, the system shows better resistance to transient faults, noise, and hardware degradation, which are common in harsh operating environments. Although TMR increases hardware complexity, area, and power consumption, the improvement in system dependability outweighs these drawbacks. Overall, the results confirm that TMR is an effective and practical approach for enhancing the fault tolerance of microcontroller-based digital systems, especially in safety-critical and real-time applications where reliability is a primary concern.

3.2. Discussion

The development of a fault-tolerant digital system using Triple Modular Redundancy (TMR) in microcontroller components is important for applications requiring high reliability and continuous operation. TMR is a widely used fault-tolerant technique in digital systems. By triplicating a system or component and using a majority voting system, TMR ensures that the system remains operational even in the event of failure. In this approach, critical microcontroller components such as the arithmetic logic unit, control unit, registers, timers, and memory interfaces are replicated three times and operate in parallel with the same input signals. The outputs of these identical components are compared using a majority voter, which selects the correct output based on a two-out-of-three decision. If one component fails due to hardware faults, noise, or environmental effects, the remaining two components continue to provide the correct output, thereby masking the fault. This ensures uninterrupted system operation and improves reliability in safety-critical applications such as aerospace, automotive, and medical systems. Although TMR increases hardware cost, power consumption, and design complexity, it offers a highly effective solution for developing fault-tolerant microcontroller-based digital systems where failure is unacceptable. - TMR can be used in systems that require high reliability and fault tolerance, such as navigation and communication systems. TMR can be used in safety-critical systems, such as airbag control systems and autonomous vehicles. Emerging Technologies: TMR can be applied to emerging technologies like AI and IoT to improve their reliability and fault tolerance (Figure 1).

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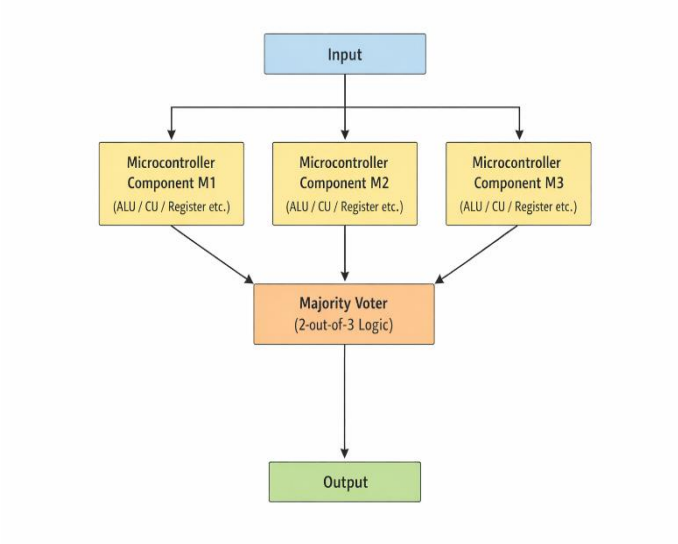

Figure 1 Block Diagram of Fault Tolerant Digital System

Conclusion

The project demonstrates that Triple Modular Redundancy (TMR) is an effective technique for enhancing the reliability and availability of digital systems operating in fault-prone or safety-critical environments. By triplicating the critical logic and introducing a majority voter, the implemented system is able to tolerate single-module faults while preserving correct functional behaviour under normal and faulty conditions. Experimental evaluation and fault-injection tests confirm that the TMR architecture successfully masks single faults with acceptable overhead in terms of area and timing, making it suitable for applications where uninterrupted and correct operation is more important than minimal resource usage. Overall, the work validates TMR-based design on Micro controller as a practical and robust approach for implementing fault-tolerant digital systems and provides a foundation for future improvements such as optimized voter circuits or selective (partial) redundancy for further resource savings.

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Fault tolerance is an essential requirement in digital systems used in safety-critical and mission-critical applications. Triple Modular Redundancy (TMR) is a widely adopted fault-tolerant technique in which three identical modules operate in parallel, and a majority voter determines the final system output, thereby masking single module faults. Kastensmidt *et al.* [1] investigated the optimal design of TMR logic for SRAM-based microcontrollers. Their work focuses on improving system reliability while reducing hardware overhead. The study demonstrates that TMR effectively mitigates single [event upsets (SEUs) and transient faults, making it suitable for high-reliability environments. In [2], a microcontroller-based TMR architecture was implemented for digital pulse width modulation (PWM) applications. The authors showed that the proposed TMR system maintains correct output operation even in the presence of faults in one of the redundant modules, thus enhancing system reliability in real-time digital control applications. A fault-tolerant triple modular system using a microcontroller was presented in [3]. This work emphasizes practical implementation and experimental validation of TMR. The results confirm that the system can tolerate single module failures without affecting overall system functionality. Based on the reviewed literature, it is evident that TMR is an effective and reliable technique for improving the fault tolerance of digital and microcontroller-based systems. These studies provide strong motivation for implementing TMR in the proposed digital system.

References

[1]. F. Lima Kastensmidt, L. Sterpone, L. Carro, and M. Sonza Reorda, “On the Optimal Design of Triple Modular Redundancy Logic for SRAM-based Micro controller”, arXiv

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https://doi.org/10.47392/IRJAEH.2026.0100

preprint arXiv:0710.4688, 2007.arxiv

[2]. "Micro controller based Design of Triple Modular Redundancy for Digital Pulse Width Modulation," Revista Geintec, vol. 12, no. 3, 2022.revistageintec

[3]. "Fault Tolerant Triple Modular System Using Micro controller," Biotechnology and Biochemistry Research Communications (BBRC), Special Issue, 2021.bbrc