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A New Configuration of Nine Level Switched Capacitor Boost Inverter of Single DC Source with Reduced Component Count

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Abstract
Renewable energy applications have shown a strong interest in switched-capacitor (SC) based multilevel inverters (MLIs) because of their ability to raise ac voltage while simultaneously balancing the capacitor's voltage. It is less expensive and takes up less space than other topologies since it just uses one source. New switched-capacitor multilevel inverters (SCMLIs) have been developed in effect to expanding demands for higher power capacities with enhanced power quality. Recently designed SCMLIs let for maximize ac output via inversion with single-stage voltage enhanced. In an attempt to decrease the quantity of apparatus, this study presents a nine-level SCMLI that utilize two capacitors with three diodes, and is of the boost kind. Voltages across capacitors are balanced by design and may be quadrupled starting a single source when using the series-parallel connection method. No semiconductor device can withstand voltage stresses extra than double the input voltage. The suggested SCMLI may be upgraded to handle higher voltage levels with fewer components and no extra dc input. Each expansion module keeps the maximum voltage stress constant at 9 levels, but adds 2 more steps to the output voltage. After a comprehensive estimate of power losses with circuit functioning, a study of recently planned single-phase 9-level MLIs is conducted to validate their design is better. In regulate to validate the key individuality of the 9-level SCMLI in real-time prepared environments, widespread simulation results are provided. For the purpose of determining if the new multi-level inverter was feasible, the analysis and simulation waveforms were evaluated under a range of load circumstances. The performance of the suggested MLI is superior to that of current multilayer inverters.
***Keywords:** Multilevel Inverter, Switched Capacitor, Novel Design, Reliability, Reduced Component Count.*

1. Introduction
The conventional construction of a multilevel inverter, which finds widespread application in areas such as renewable energy production and industrial drive systems, involves an input source with a half H-bridge layout. Reduced operational switches and less voltage blocking between the switches are two benefits of decreased switch topologies, whether they are symmetrical or asymmetrical, in the context of multilevel inverters [1]-[3]. Modern high-power and medium-voltage manufacturing processes, especially those involving renewable energy sources and grid connectivity, have seen a dramatic rise in the need for multilayer inverters (MLIs). Minimal-voltage-rated switching devices, less dv/dt, little electromagnetic distortion, and large-power processing capacity are a few of the ways in which MLIs outperform traditional two-level inverters. Cascaded h-bridge (CHB) MLIs, neutral-point-clamped (NPC) MLIs, and flying-capacitor clamped (FCC) MLIs are the three most common kinds of MLLs employed in this field [4]-[6]. But there are a lot of capacitors and power switches needed for these topologies. In addition, the CHB needs a number of separate DC sources. Capacitor equilibrium in the NPC and FCC, particularly at advanced stage generation, requires complex control schemes and/or extra circuitry. It is possible to minimize the number of components in a hybrid inverter by utilizing topologies that are developed from classical topologies [7]. In an effort to create structures that utilize the fundamental voltage boosting SC method, which might be beneficial for PV applications, we suggest generalized MLIs. The basic module of the generalized MLI that was published has a single

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source, a single capacitor, a single diode, and two switches. These switches allow the capacitor, which helps with the inherent voltage increase, to be charged and discharged. Extending this architecture in both symmetrical and asymmetrical directions necessitates a substantial amount of switches [8]-[10]. Because it uses series diodes, the single-dc MLI can't function when the power factor (PF) is low. Two diodes and two capacitors make up the front-end design of the nine-level single-input MLI that is demonstrated. The circuit's capacitors are stimulating to partially the amount of the input voltage, limiting voltage boosting to twice the input. The TVS is further enhanced in these topologies by including an H-bridge into the backend [11]-[12]. Thus, new generalized MLIs were suggested without the need for a complete bridge at the back end. To get larger voltage levels at the output, though, you'll need a combination of symmetrical and asymmetrical sources [13]. The goal of the generalized circuit architecture is to decrease the amount of capacitors. Nevertheless, it is unable to circumvent the need for several sources. Using an individual dc source with a minimum quantity of capacitors, 9-level MLIs are built to overcome this issue. At most, the voltage gain can only be twice as large as the input voltage in this case. Significant step-up single-input SCMLIs have also been reported in recent literature [14]. The structure drastically lowers voltage stress and may be expanded to provide larger voltage levels, but it requires a lot of switches. The generic circuit drastically cuts down on the amount of switches. But there are a few of switches that are rated for max output voltage [15]. Both 9-level double boost MLIs and 10-level MLIs with the same number of switches are suggested; however, the former uses three capacitors while the latter uses two. Reduced switch count is a major benefit of the described circuit. The three capacitors used are comparable to the MLI, and two of the transistors have a max output voltage rating. There has been talk of a 9-level MLI, and to implement it, four switches rated for peak output voltage are necessary [16]-[21]. This study suggests a simplified switch SCMLI with some of its salient characteristics, all while keeping in mind the shortcomings of the current 9-level structures: 1) to get a 9-level quadratic boost output, you need one input source and 10 switches. 2) With no further control complexity, inherent voltage balancing capabilities. 3) Every switching device are rated at their lowest possible voltage, which is double the input voltage; no switches are rated for max output voltage. 4) Workability under temporary loads is satisfactory.

2. Proposed System

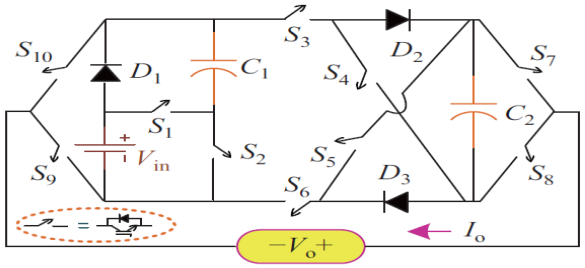

Figure 1 9-level SCMLI Proposed Topology

Figure 1 shows the suggested 9-level single-phase SCMLI with one dc supply (Vin) and ten switches (S1-S10). The circuit may be broken down into two halves for easier examination. Two switches (S1, S2), one diode (D1), and one capacitor (C1) make up the first module (M1), whereas four switches (S3-S6), two diodes (D2, D3), and one capacitor (C2) make up the second module (M2). The input voltage is doubled by the M1, and its output is further doubled by the M2. Bypassing the end-side complete bridge, the switches (S7–S10) are configured to generate the necessary ac output. Therefore, the stress across all of the strategy in M1 is Vin, whereas all of the other apparatus can sustain stress levels of 2Vin. The suggested MLI generates a 9-level output (0, ±Vin, ±2Vin, ±3Vin, ±4Vin) by keeping the voltage ratio of 1:2 between capacitors C1 and C2. The following pairs of switches (S1, S2), (S3, S5), (S4, S6), (S7, S8), and (S9, S10) simplify the functioning of the topology because they work in tandem. Moreover, in order to avoid source short circuiting, it is not allowed to operate (S3, S4, S6) & (S3, S5, S6) switch combinations simultaneously. Only if switch S1 is turned off is diode D1 forward biased; when switch pairs S4 and S5 are turned off, diode D2 as well as D3 are also forward biased. Moving further, we will examine the performance analysis of the suggested

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design while ignoring the voltage drop between semiconductor devices and considering that capacitors can maintain an equilibrium voltage in the ratio Vin: 2Vin. Capacitor C1 is discharged with capacitor C2 is stimulating when Vo = 0, since S1 from M1 & S3&S6 from M2 are in a conduction condition. Switch pairs (S8, S9) with (S7, S10), when turned on simultaneously, provide a zero-level output. While Vo =±Vin, capacitor C1 is charged by the conduction of switch S2. During the positive half-cycle, switches (S3, S4, S8, S9) are also switched on, and during the negative half-cycle, switches (S5, S6, S7, S10) are turned on. C2 is a static capacitor. The conduction states of the switches from both M1 and M2 are comparable to the zero-level when Vo = ±2Vin. In a series of voltage steps, the polarity may be reversed with the help of switch pairs (S7, S9) & (S8, S10). Conduction from Switch S2 charges Capacitor C1 when Vo = ±3Vin. By cycling through the positive with negative half-cycles of switch pairs (S3, S4) & (S5, S6) from M2, respectively, C2 is discharged in sequence with the component. The operation is identical to the previous level, with the exception that switch S1 is now conducting, enabling the discharge from the two capacitors in line with the source, and the peak output is ±4Vin.

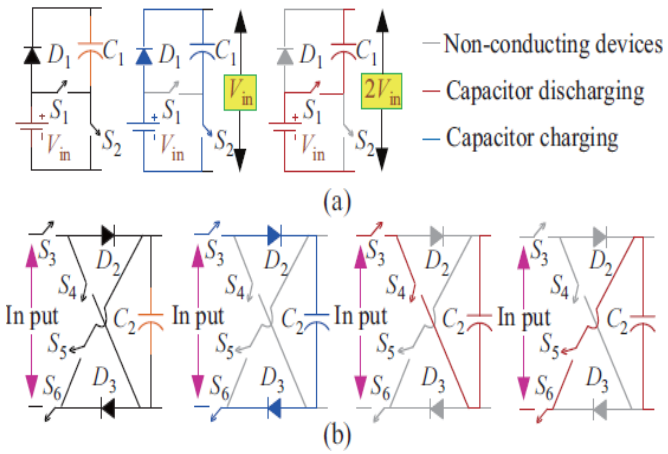

Figure 2 Analysis of SCs Charging & Discharging

The charging-discharging processes of SCs C1 and C2, respectively, are illustrated in Figure 2(a) and 2(b). At ±Vin and ±3Vin, C1 charges in parallel with the input supply, as shown in Figure 2, while at other instants, it discharges in sequence with the source. This means that the voltage across C1 remains constant at its steady-state value. Conversely, when M1's output is 2Vin, C2 is charged between zero and ±2Vin in tandem with it. Between ± 3Vin and ± 4Vin, it discharges in series with M1's output. Because to the basic cycle's regular charging and discharging, an equilibrium voltage of 2Vin remains stable across C2. Capacitor voltages remain at the correct level regardless of loading because (a) the instance it considers to charge with discharge is significantly fewer than the entire output voltage period and (b) the route have a low parasitic resistance.

3. Simulation Results

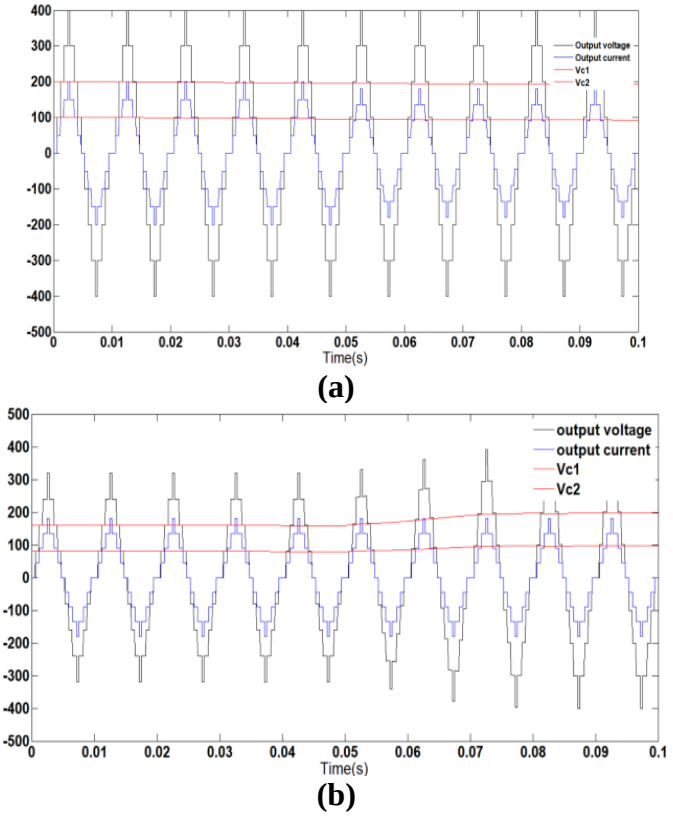

Figure 3 Proposed System, (a) Output Voltage, Current and Capacitor Voltages Under Variation in Modulation Index (M=0.95 to M=0.3) (b) Sudden Variation in DC input. (Inductive load)

Using a basic frequency switching approach that is based on pre-computed angles, switching pulses is created. To begin, we connect the suggested circuit to Load 1 and measure the output with different values

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of M. Figure 3(a) shows that the 9-level voltage at load waveform is indistinguishable from the load current arrangement when subjected to pure resistive loading. There is no change to the essential value even when M = 0.95. There is no additional voltage balancing control used to keep the capacitor voltages at 100 V and 200 V, respectively. We also test the suggested circuit under dynamically changing inductive loads to make sure it works. Under a quick load transient, the capacitor voltages remain at the appropriate value, which helps in synthesizing the 9-level quadruple boost output, which is around 400 V. Additionally, as shown in Figure 3(b) for an abrupt modify in the input dc voltage, the capacitor voltages logically settle to the correct level behind a slow adjustment.

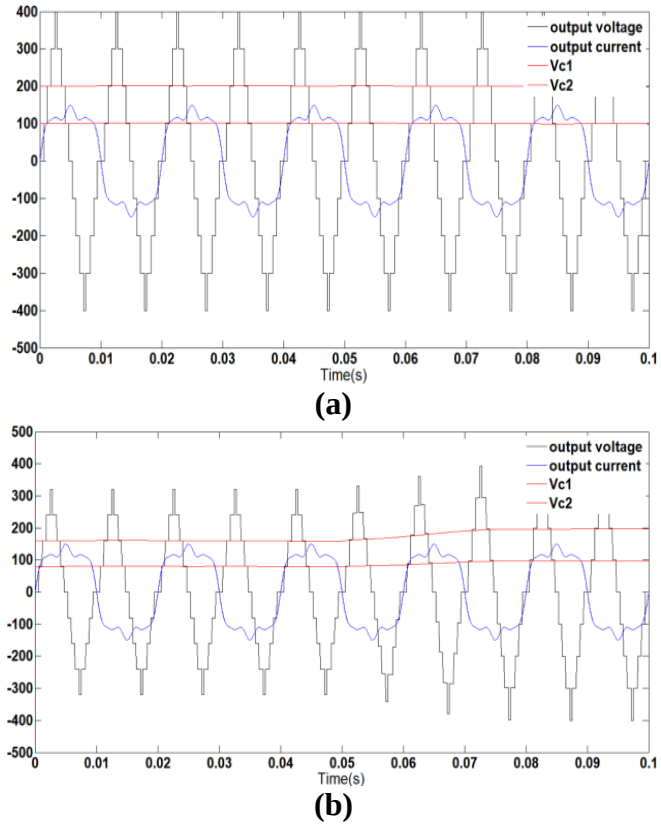

Figure 4 Proposed System, (a) Output Voltage, Current and Capacitor Voltages Under Variation in Modulation Index (M=0.95 to M=0.3) (b) Sudden Variation in DC input. (PMSM)

In Figure 4 shows the proposed waveforms with permanent magnet synchronous machine act as a load. When compared with inductive load, the current waveforms are changes in the PMSM load conditions.

Conclusion

A 9-level SCMLI of the boost type with a reduced amount of parts and two SCs was introduced in this study. The steady-state voltage between the SCs is kept at Vin and 2Vin by charging them in parallel as well as discharging them in series. Because of this, the suggested MLI simplifies handling by eliminating the need for an auxiliary voltage balancing circuit. Furthermore, the ac output is generated not including the use of a traditional full-bridge, which greatly reduces voltage stress and limits MVS to 2Vin. No material how far the topology is extended, the amount of dc sources with the MVS stay constant. Because of these unique characteristics, the suggested SCMLI works well in PV systems that only have one stage. The studies of power loss, operational concepts, and the charging-discharging process have all been covered extensively. The suggested SCMLI manages to save costs significantly while keeping all the other benefits, according to a comprehensive comparison study.

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